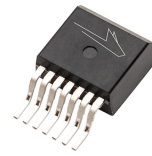


C3M0045065J1

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology
N-Channel Enhancement Mode

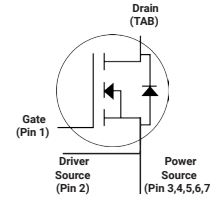


TO-263-7L XL



Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant



Package Types: TO-263-7L XL
PN's: C3M0045065J1

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Typical Applications

- Datacenter and telecom power supplies
- EV battery chargers
- High voltage DC/DC converters
- Energy storage systems
- Solar inverters

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			47	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Fig. 19 Note 2
				31		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 150^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			132		t_{pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			147	W	$T_c = 25^\circ\text{C}, T_J = 150^\circ\text{C}$	Fig. 20
Operating Junction Temperature	T_J			-40 to +175	$^\circ\text{C}$		
Case and Storage Temperature	T_c, T_{stg}			-40 to 150			
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


Electrical Characteristics ($T_C = 25^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650				$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.6	3.6	V	$V_{DS} = V_{GS}, I_D = 4.84\text{ mA}$	Fig. 11
			2.3			$V_{DS} = V_{GS}, I_D = 4.84\text{ mA}, T_J = 150^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}		1	50	μA	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	I_{GSS}		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$		45	60	m Ω	$V_{GS} = 15\text{ V}, I_D = 17.6\text{ A}$	Fig. 4, 5, 6
			54			$V_{GS} = 15\text{ V}, I_D = 17.6\text{ A}, T_J = 150^\circ\text{C}$	
Transconductance	g_{fs}		12		S	$V_{DS} = 20\text{ V}, I_{DS} = 17.6\text{ A}$	Fig. 7
			11			$V_{DS} = 20\text{ V}, I_{DS} = 17.6\text{ A}, T_J = 150^\circ\text{C}$	
Input Capacitance	C_{iss}		1621		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 400\text{ V}$ $f = 1\text{ MHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
Output Capacitance	C_{oss}		101				
Reverse Transfer Capacitance	C_{rss}		8				
Effective Output Capacitance (Energy Related)	$C_{o(er)}$		126			$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 400\text{ V}$	Note: 2
Effective Output Capacitance (Time Related)	$C_{o(tr)}$		178				Note: 2
C_{oss} Stored Energy	E_{oss}		10		μJ	$V_{DS} = 400\text{ V}, f = 1\text{ MHz}$	Fig. 16
Turn-On Switching Energy (Body Diode)	E_{ON}		36		μJ	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 17.6\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 99\text{ }\mu\text{H}, T_J = 25^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
Turn-Off Switching Energy (Body Diode)	E_{OFF}		7				
Turn-On Delay Time	$t_{d(on)}$		8		ns	$V_{DD} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 17.6\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 99\text{ }\mu\text{H}$ Timing Relative to V_{DS} Inductive Load	Fig. 26
Rise Time	t_r		10				
Turn-Off Delay Time	$t_{d(off)}$		19				
Fall Time	t_f		6				
Internal Gate Resistance	$R_{G(int)}$		3		Ω	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	Q_{gs}		21		nC	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 17.6\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}		16				
Total Gate Charge	Q_g		61				

Note (2): $C_{o(er)}$, a lumped capacitance that gives same stored energy as c_{oss} while V_{DS} is rising from 0 to 400 V.

$C_{o(tr)}$, a lumped capacitance that gives same charging time as c_{oss} while V_{DS} is rising from 0 to 400 V.

Reverse Diode Characteristics (T_c = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V _{SD}	4.8		V	V _{GS} = -4 V, I _{SD} = 8.8 A, T _J = 25 °C	Fig. 8, 9, 10
		4.2			V _{GS} = -4 V, I _{SD} = 8.8 A, T _J = 150 °C	
Continuous Diode Forward Current	I _S		26	A	V _{GS} = -4 V, T _C = 25 °C	
Diode Pulse Current	I _{S, pulse}		132		V _{GS} = -4 V, Pulse Width t _p Limited by T _{Jmax}	
Reverse Recovery Time	t _{rr}	10		ns	V _{GS} = -4 V, I _{SD} = 17.6 A, V _R = 400 V dif/dt = 5420 A/μs, T _J = 25 °C	
Reverse Recovery Charge	Q _{rr}	206		nC		
Peak Reverse Recovery Current	I _{rrm}	36		A		
Reverse Recovery Time	t _{rr}	13		ns	V _{GS} = -4 V, I _{SD} = 17.6 A, V _R = 400 V dif/dt = 1915 A/μs, T _J = 25 °C	
Reverse Recovery Charge	Q _{rr}	103		nC		
Peak Reverse Recovery Current	I _{rrm}	14		A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	R _{θJC}	0.85	°C/W		Fig. 21
Thermal Resistance from Junction to Ambient	R _{θJA}	40			

Typical Performance

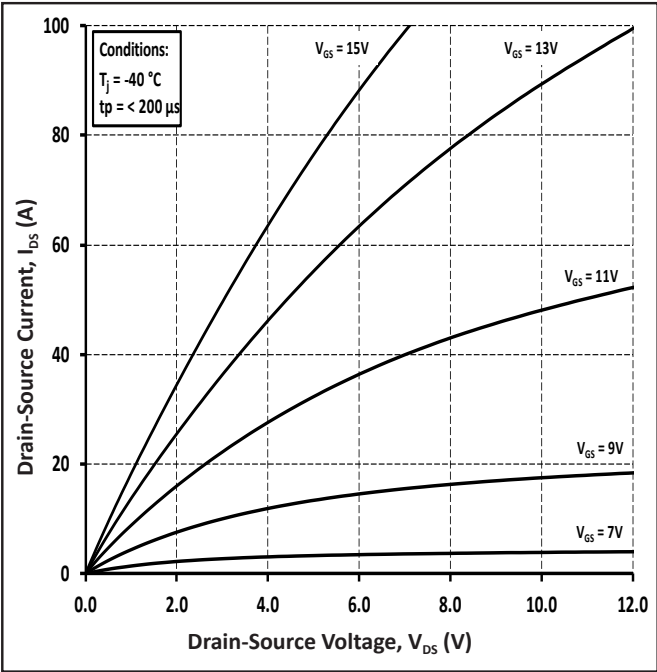


Figure 1. Output Characteristics $T_j = -40\text{ }^{\circ}\text{C}$

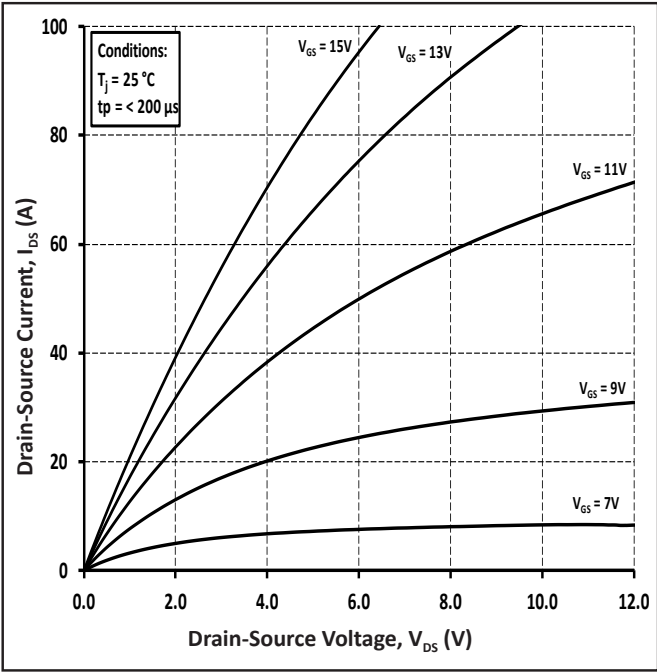


Figure 2. Output Characteristics $T_j = 25\text{ }^{\circ}\text{C}$

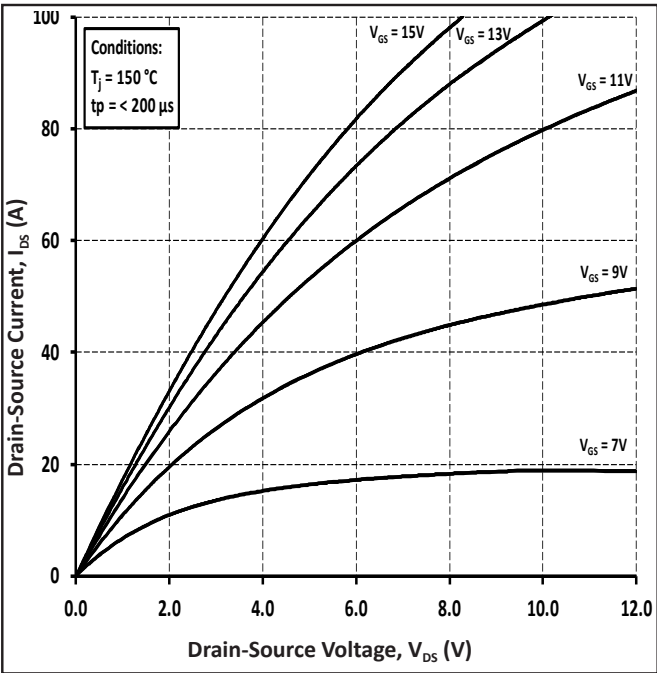


Figure 3. Output Characteristics $T_j = 150\text{ }^{\circ}\text{C}$

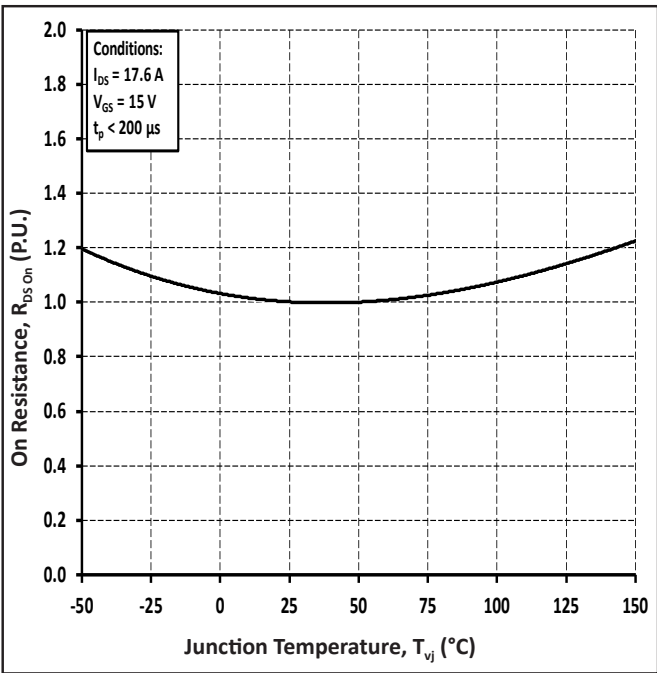


Figure 4. Normalized On-Resistance vs Temperature

Typical Performance

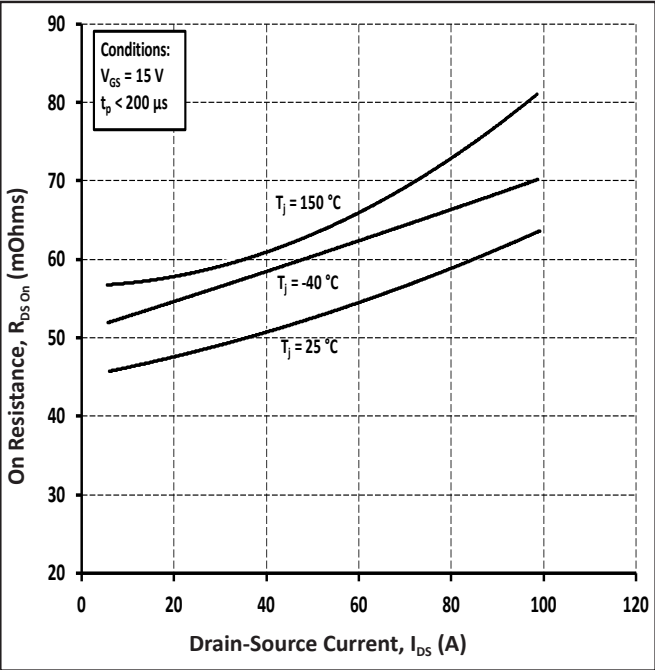


Figure 5. On-Resistance vs Drain Current for Various Temperatures

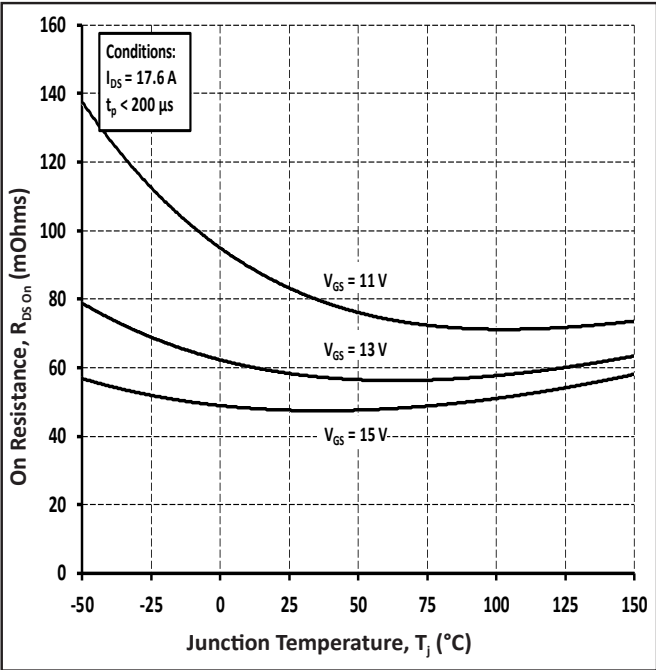


Figure 6. On-Resistance vs Temperature for Various Gate Voltage

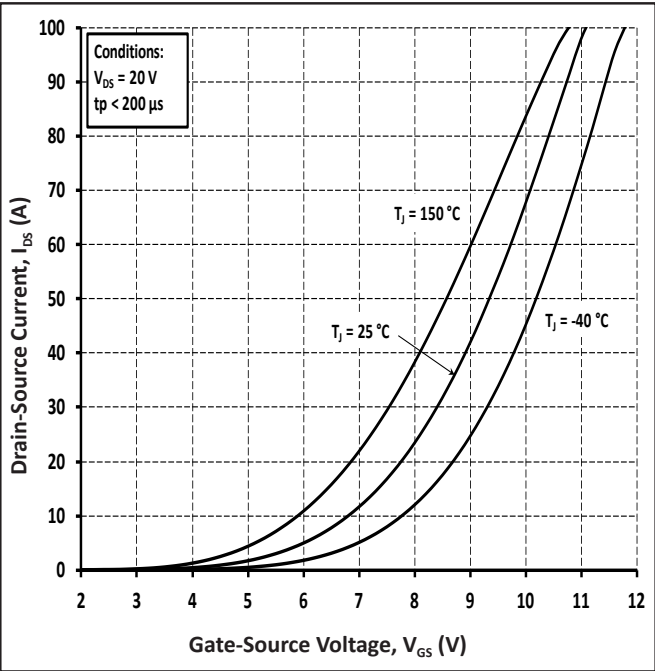


Figure 7. Transfer Characteristic for Various Junction Temperatures

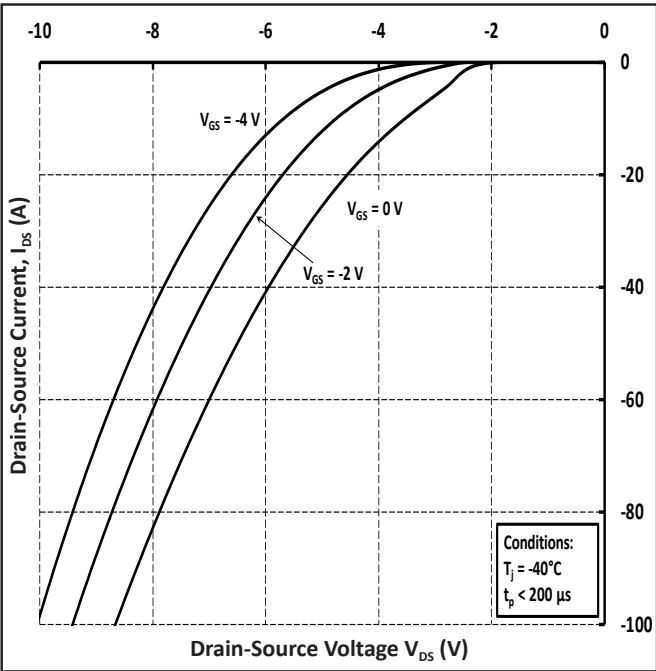


Figure 8. Body Diode Characteristic at -40 °C

Typical Performance

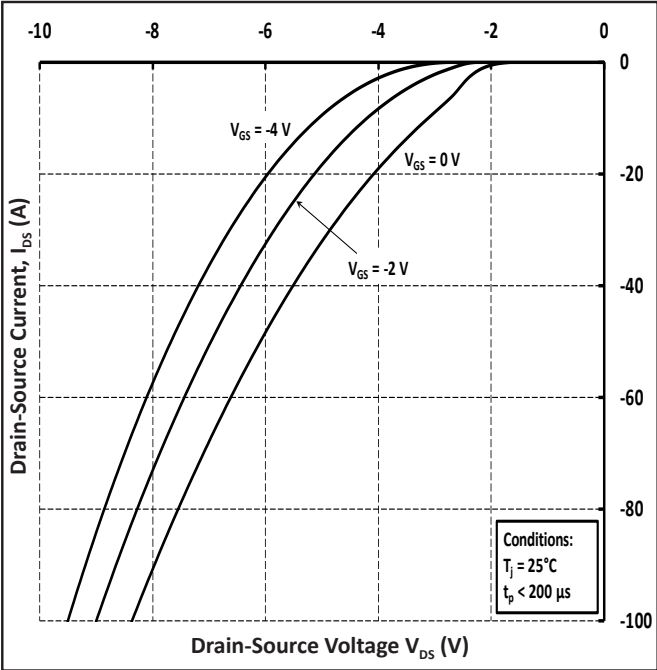


Figure 9. Body Diode Characteristic at 25 °C

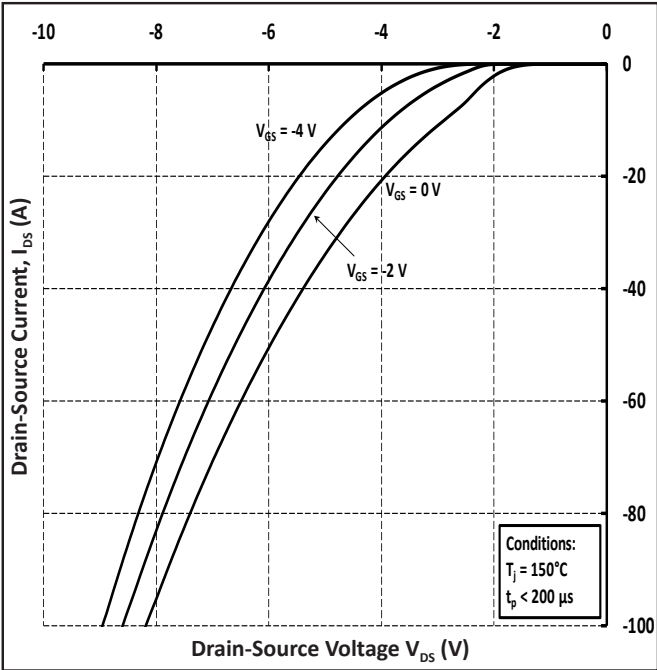


Figure 10. Body Diode Characteristic at 150 °C

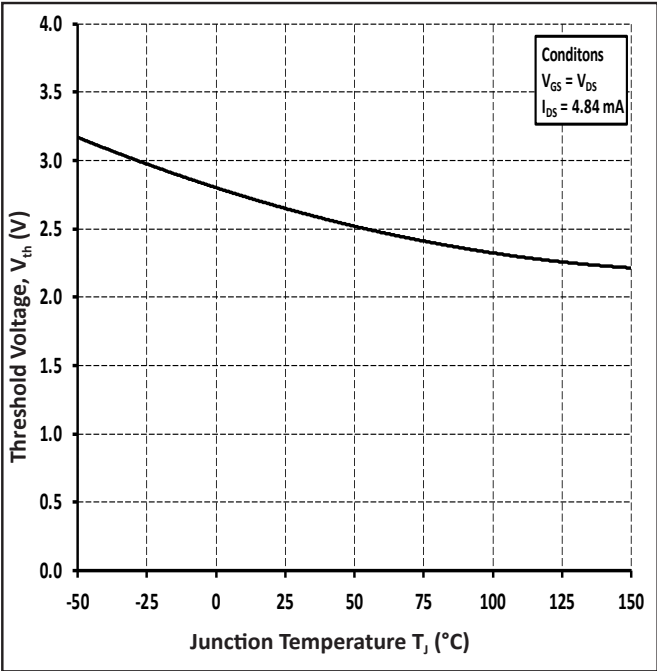


Figure 11. Threshold Voltage vs Temperature

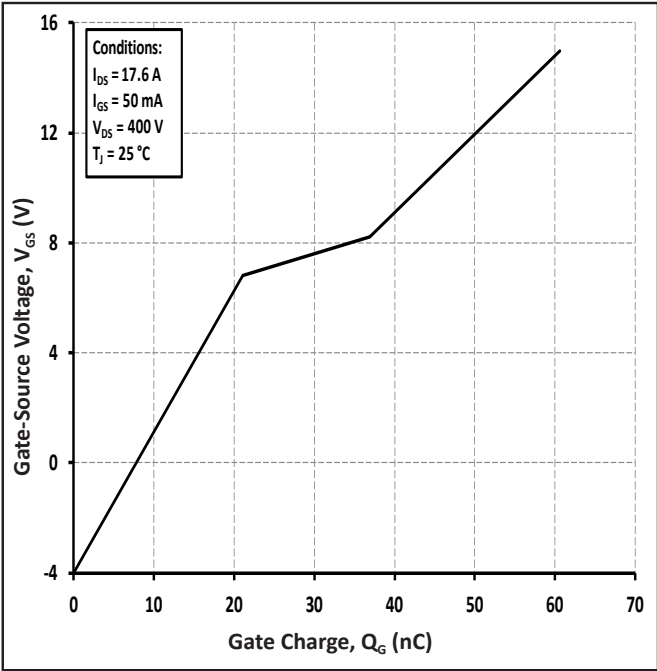


Figure 12. Gate Charge Characteristic

Typical Performance

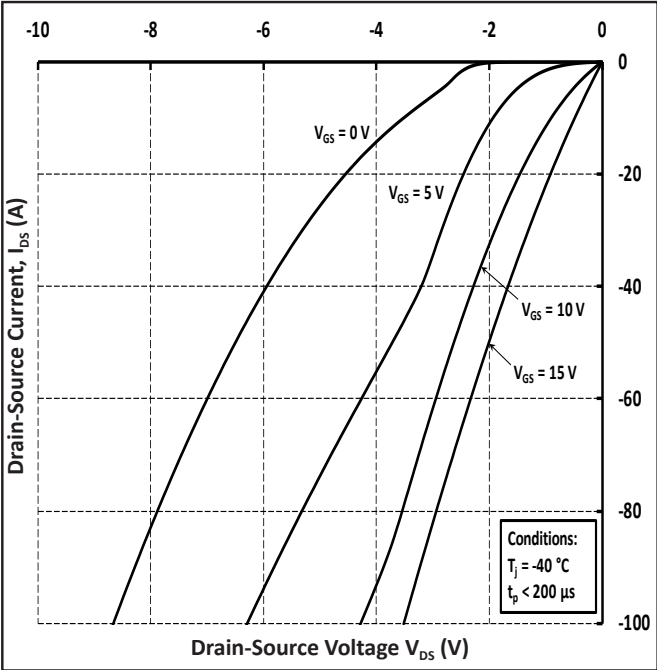


Figure 13. 3rd Quadrant Characteristic at $-40\text{ }^{\circ}\text{C}$

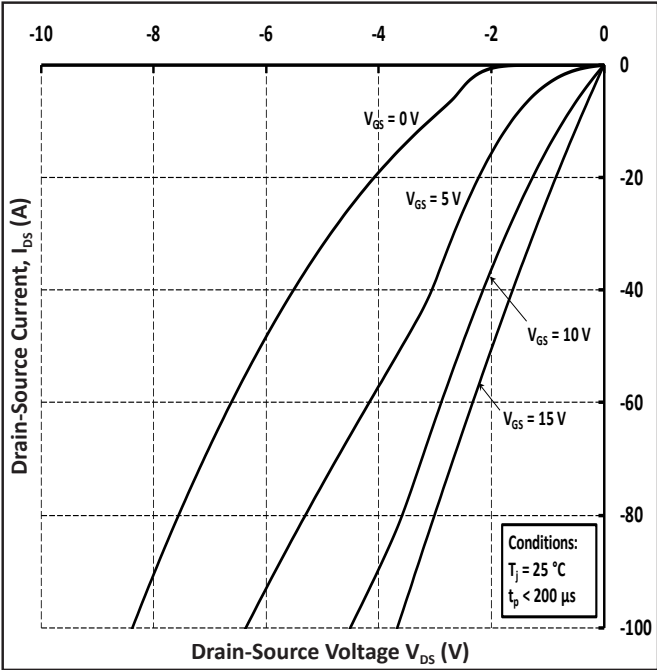


Figure 14. 3rd Quadrant Characteristic at $25\text{ }^{\circ}\text{C}$

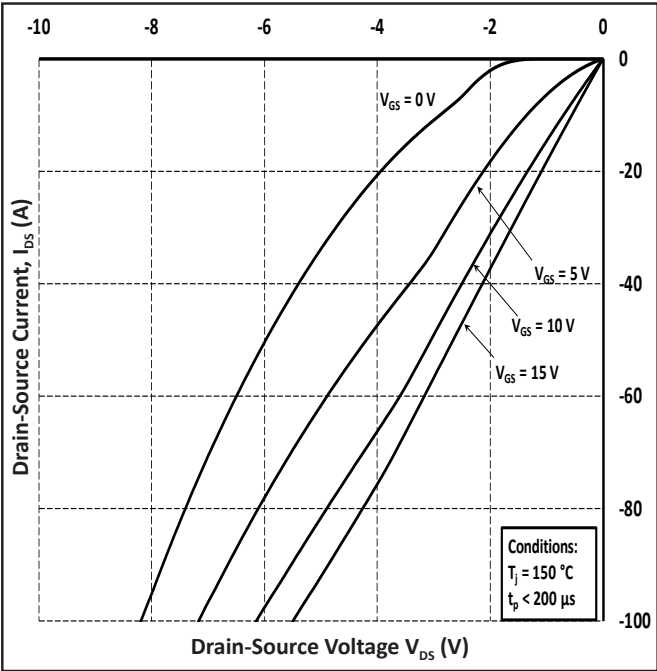


Figure 15. 3rd Quadrant Characteristic at $150\text{ }^{\circ}\text{C}$

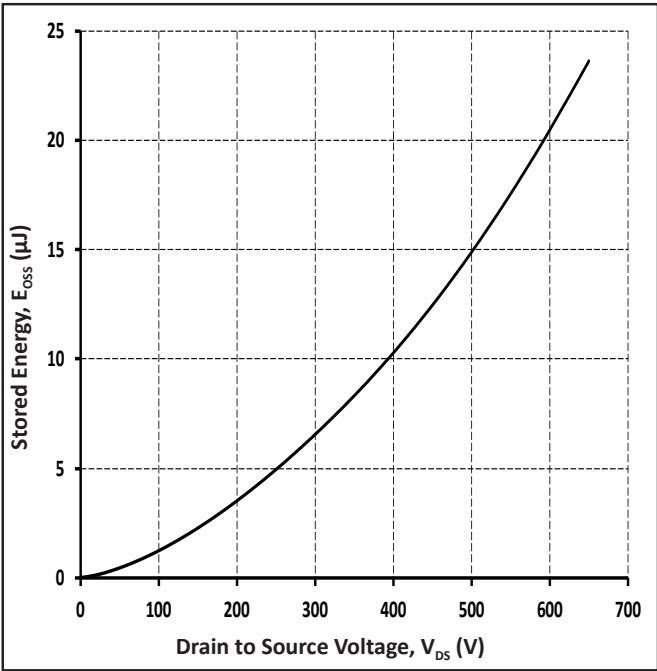


Figure 16. Output Capacitor Stored Energy

Typical Performance

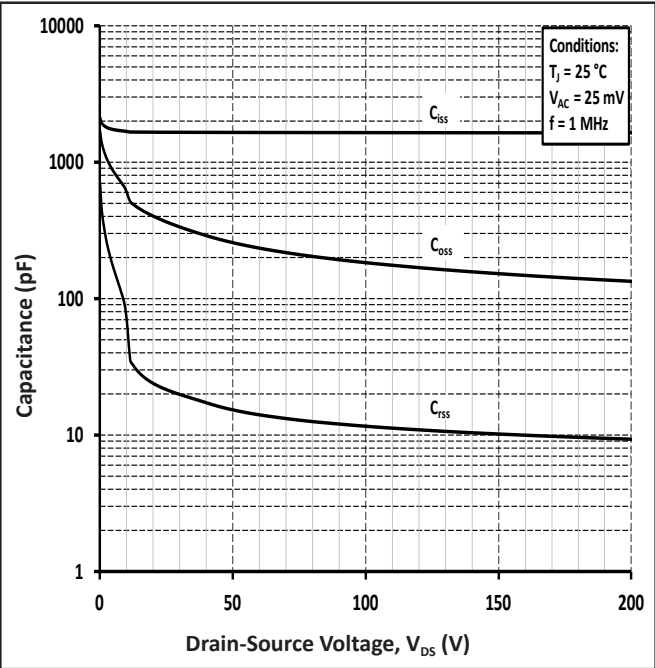


Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

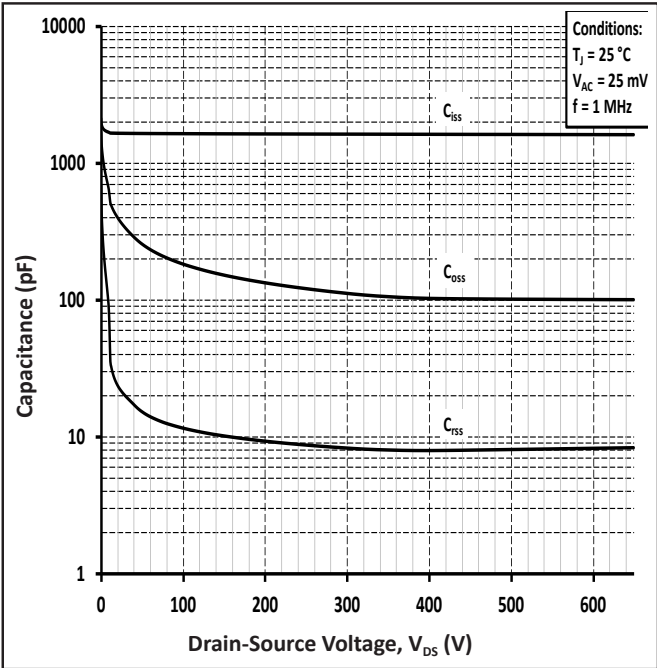


Figure 18. Capacitances vs Drain-Source Voltage (0-600 V)

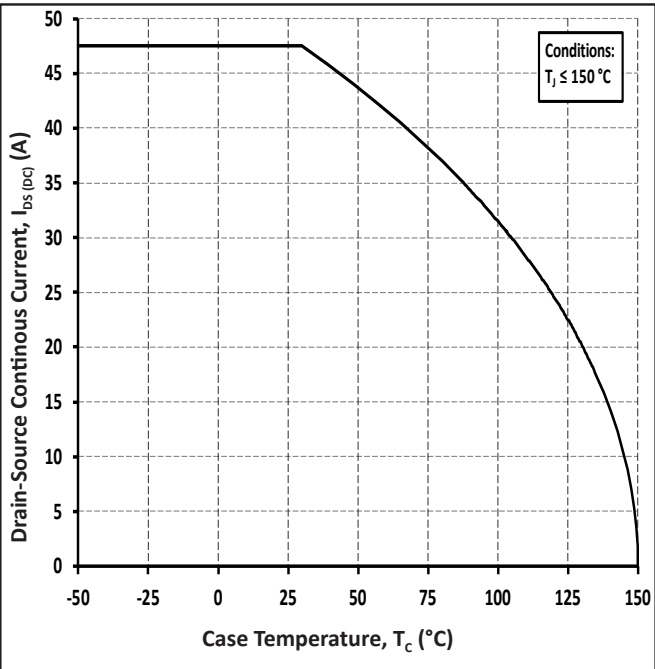


Figure 19. Continuous Drain Current Derating vs Case Temperature

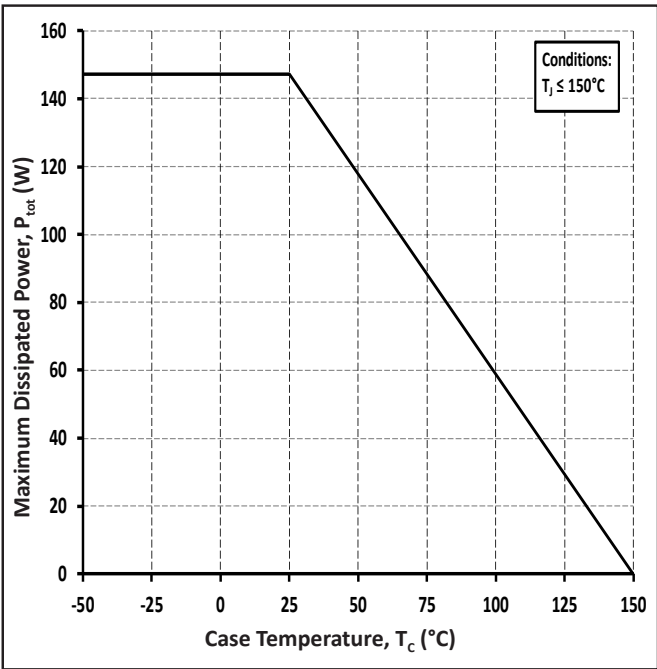


Figure 20. Maximum Power Dissipation Derating vs Case Temperature

Typical Performance

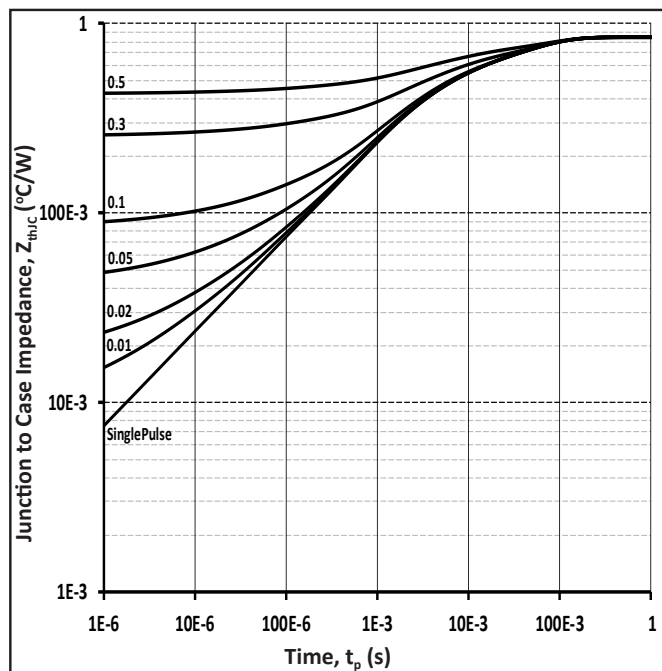


Figure 21. Transient Thermal Impedance (Junction - Case)

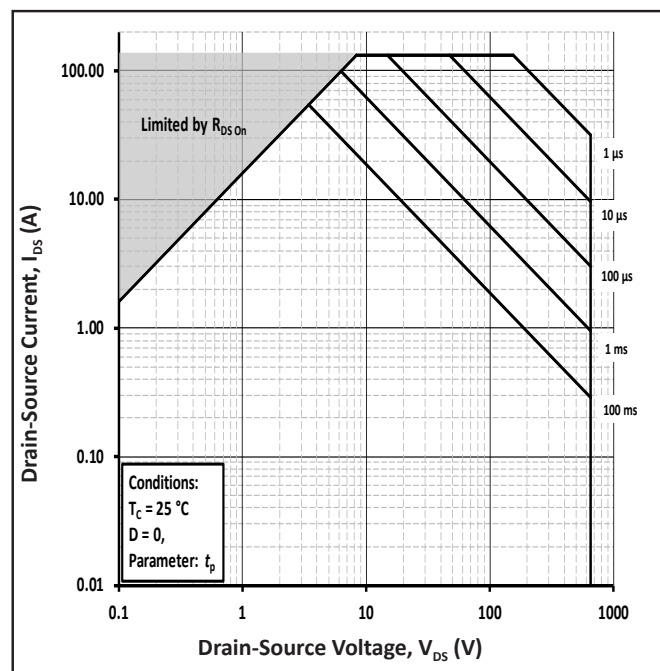


Figure 22. Safe Operating Area

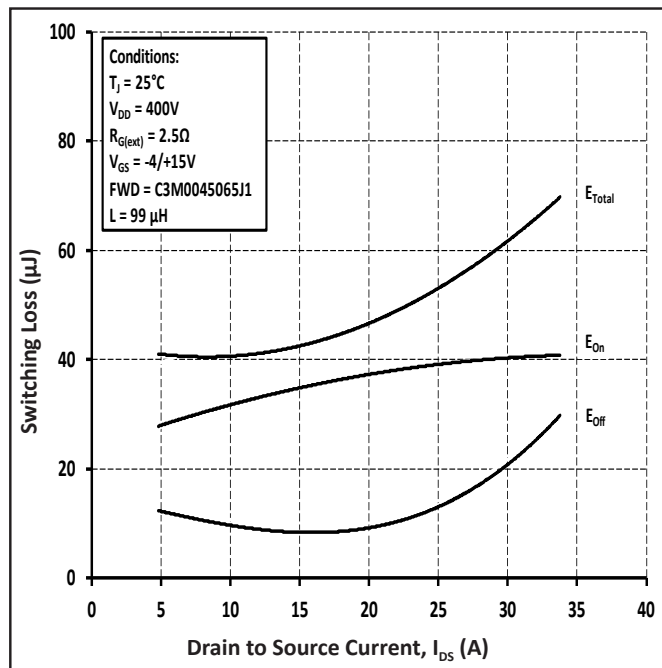


Figure 23. Clamped Inductive Switching Energy vs Drain Current ($V_{DD} = 400\text{ V}$)

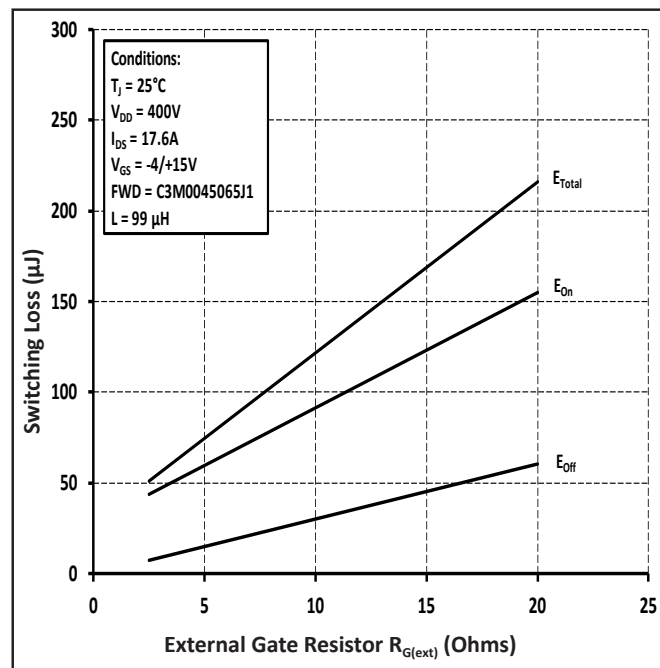


Figure 24. Clamped Inductive Switching Energy vs $R_{G(ext)}$

Typical Performance

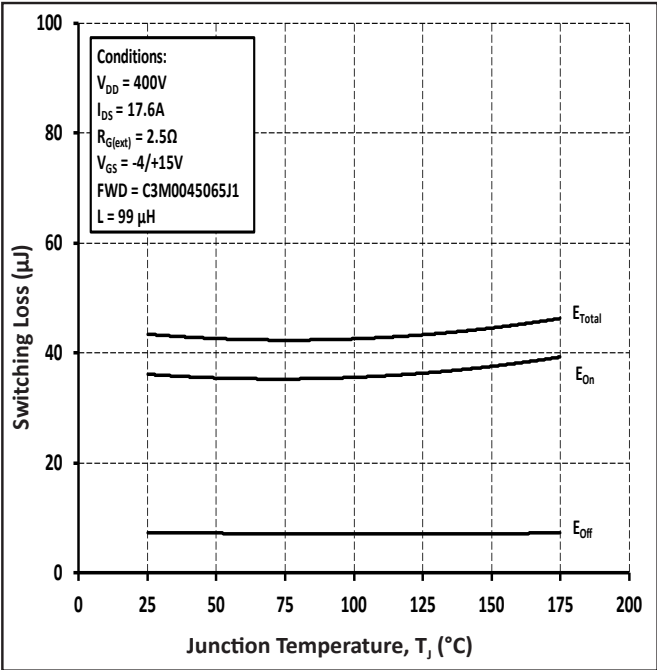


Figure 25. Clamped Inductive Switching Energy vs Temperature

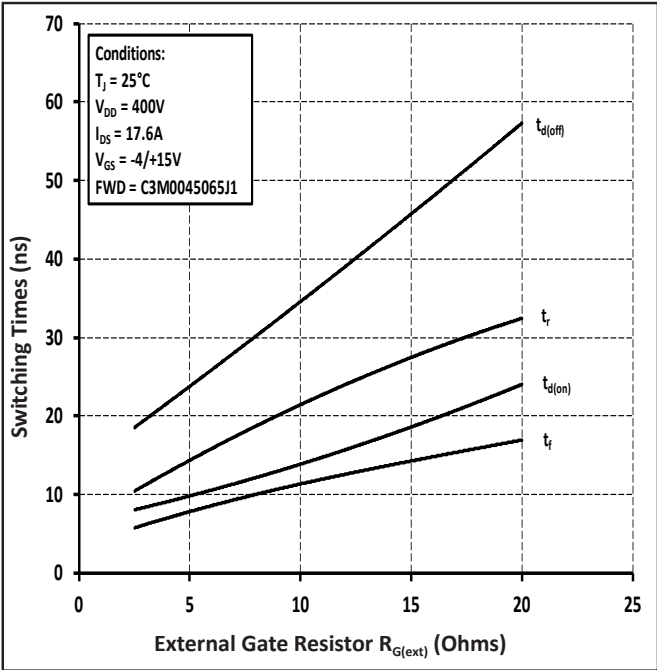


Figure 26. Switching Times vs $R_{G(ext)}$

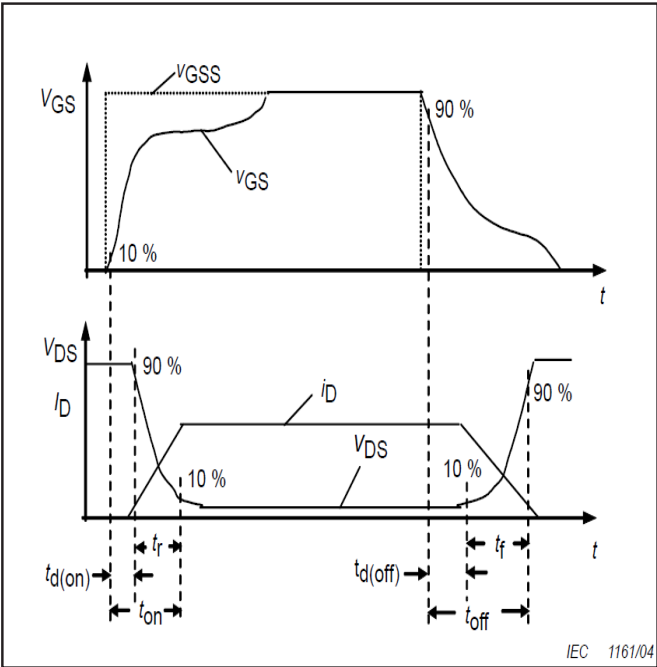


Figure 27. Switching Times Definition

Test Circuit Schematic

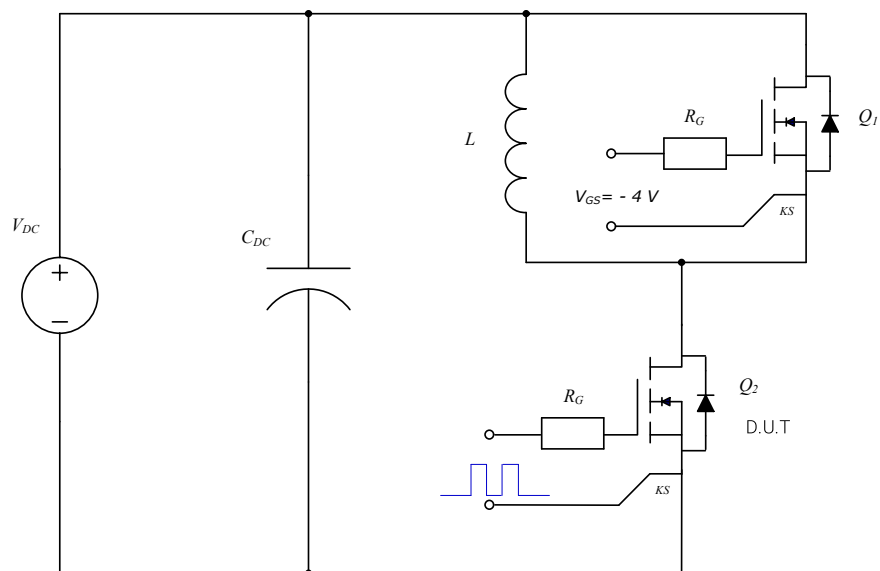
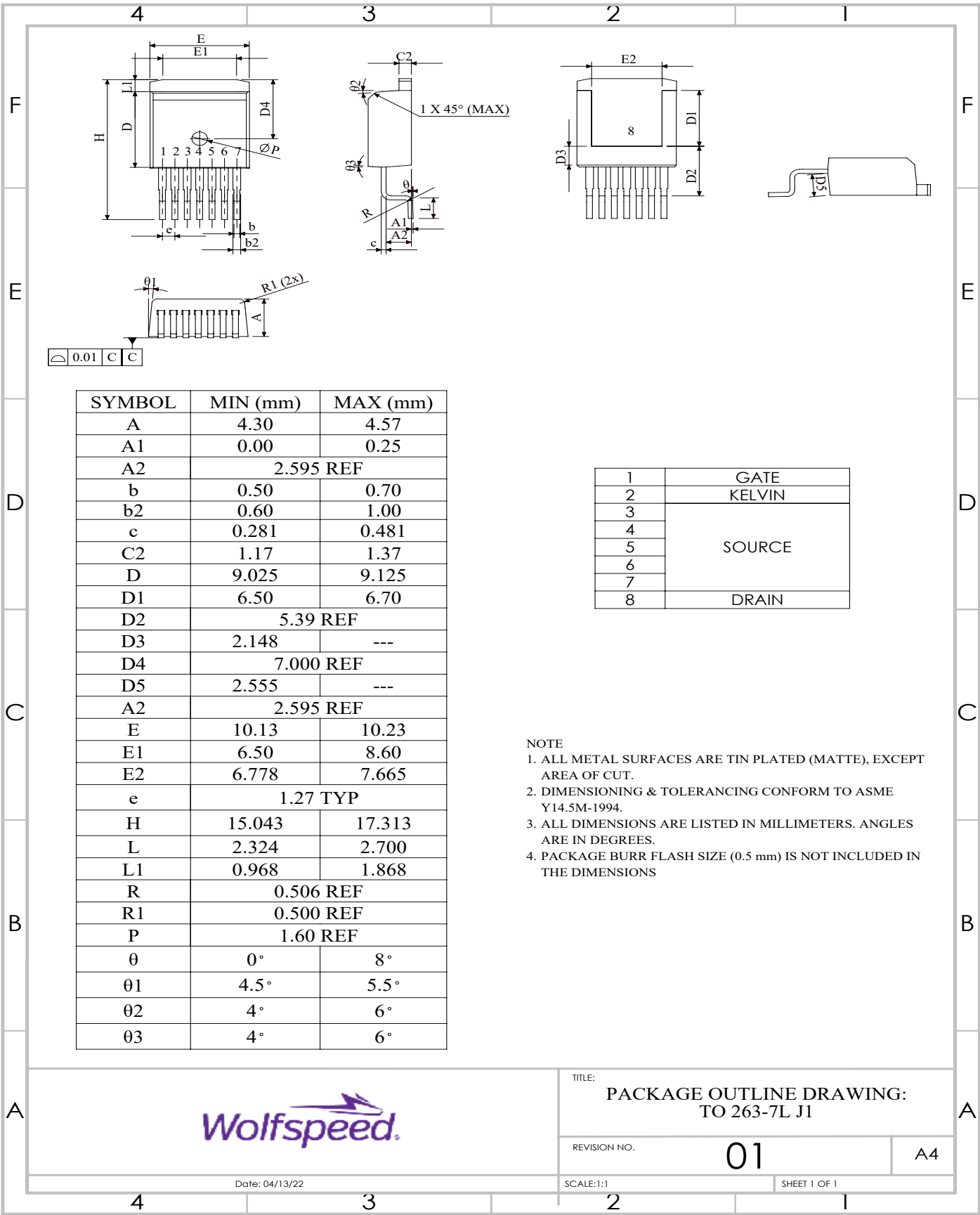


Figure 28. Clamped Inductive Switching Waveform Test Circuit

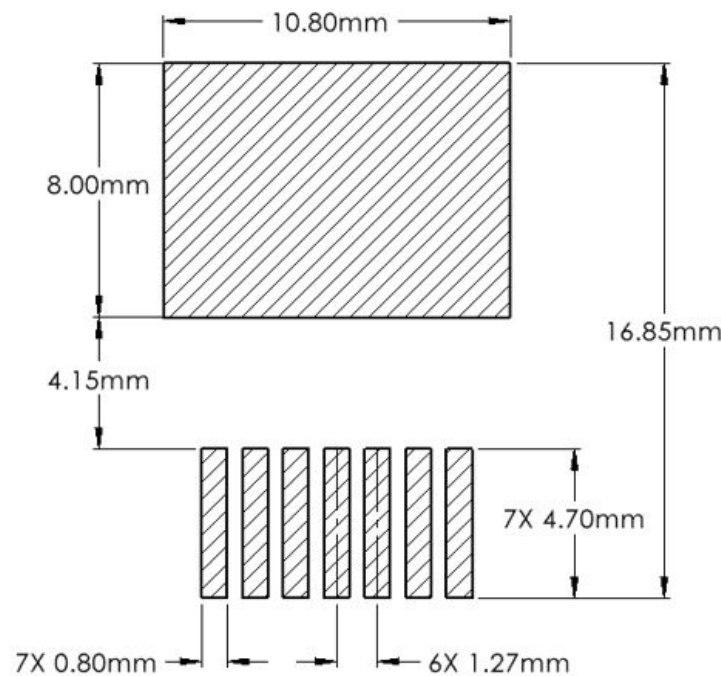
Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET body diode as shown above.

Package Dimensions

Package: TO-263-7L XL



Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
0	October-2021	N/A
1	November-2023	Updated Wolfspeed branding, package drawing, package image, solder pad layout, added revision history
2	December - 2024	Legal Disclaimer Updated



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