

EPC2106 – Enhancement-Mode GaN Power Transistor Half-Bridge

 $V_{DS}, 100\text{ V}$
 $R_{DS(on)}, 70\text{ m}\Omega$
 $I_D, 1.7\text{ A}$


Revised January 27, 2021

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:
Ask a GaN
Expert

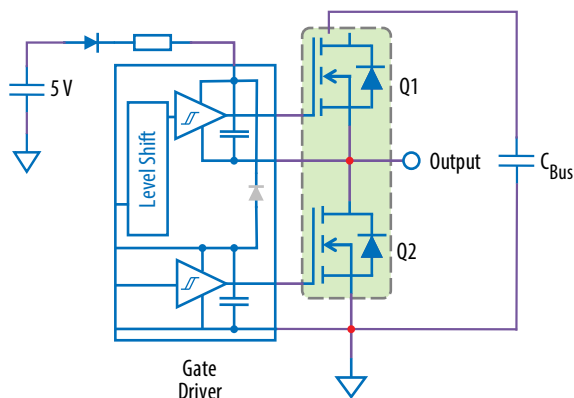


Maximum Ratings				
DEVICE	PARAMETER		VALUE	UNIT
Q1 & Q2	V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
	I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 320^\circ\text{C/W}$)	1.7	A
		Pulsed (25°C , $T_{PULSE} = 300\text{ }\mu\text{s}$)	18	
	V_{GS}	Gate-to-Source Voltage	6	V
		Gate-to-Source Voltage	-4	
	T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
	T_{STG}	Storage Temperature	-40 to 150	

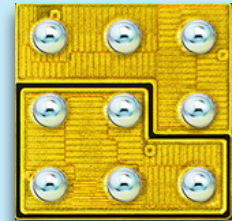
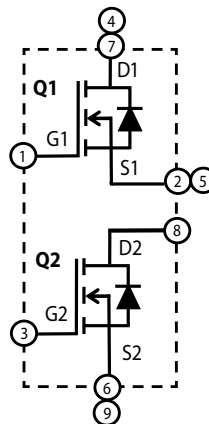
Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	30	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	81	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Typical Application Circuit



EPC2106 – Detailed Schematic



Die Size: 1.35 x 1.35 mm

EPC2106 eGaN® ICs are supplied only in passivated die form with solder bumps.

Applications

- High frequency DC-DC conversion
- Class-D audio

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!


<https://l.ead.me/EPC2106>

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1 & Q2	BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.3\text{ mA}$	100			V
	I_{DSS}	Drain-Source Leakage	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$		0.001	0.25	mA
	I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.01	1	mA
		Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.001	0.25	mA
	$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 0.6\text{ mA}$	0.8	1.4	2.5	V
	$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 2\text{ A}$		55	70	m Ω
	V_{SD}	Source-Drain Forward Voltage	$I_S = 0.35\text{ A}, V_{GS} = 0\text{ V}$		2.1		V

Dynamic Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	C_{ISS}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		79	95	pF
	C_{RSS}	Reverse Transfer Capacitance			0.5		
	C_{OSS}	Output Capacitance			52	78	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		63		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			79		
	R_G	Gate Resistance			1.3		Ω
	Q_G	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 2\text{ A}$		730	900	pC
	Q_{GS}	Gate to Source Charge	$V_{DS} = 50\text{ V}, I_D = 2\text{ A}$		240		
	Q_{GD}	Gate to Drain Charge			140		
	$Q_{G(TH)}$	Gate Charge at Threshold			165		
	Q_{OSS}	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		3960	5940	
	Q_{RR}	Source-Drain Recovery Charge			0		
Q2	C_{ISS}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		79	95	pF
	C_{RSS}	Reverse Transfer Capacitance			0.5		
	C_{OSS}	Output Capacitance			61	92	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		74		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			94		
	R_G	Gate Resistance			1.8		Ω
	Q_G	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 2\text{ A}$		730	900	pC
	Q_{GS}	Gate to Source Charge	$V_{DS} = 50\text{ V}, I_D = 2\text{ A}$		240		
	Q_{GD}	Gate to Drain Charge			140		
	$Q_{G(TH)}$	Gate Charge at Threshold			165		
	Q_{OSS}	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		4680	7020	
	Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Figure 1 (Q1 & Q2): Typical Output Characteristics at 25°C

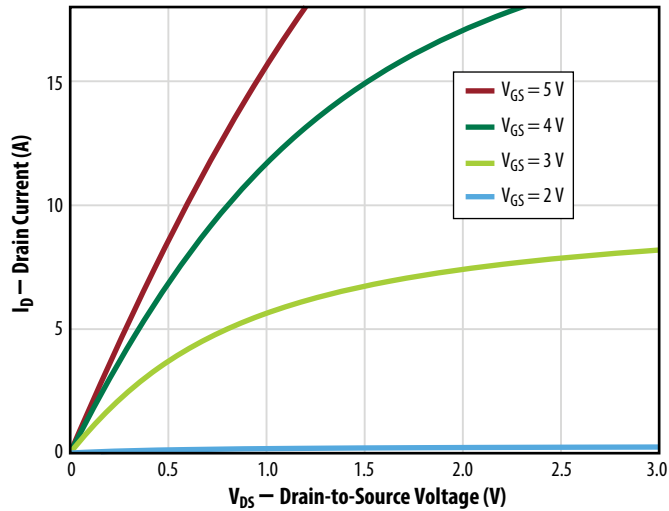


Figure 2 (Q1 & Q2): Typical Transfer Characteristics

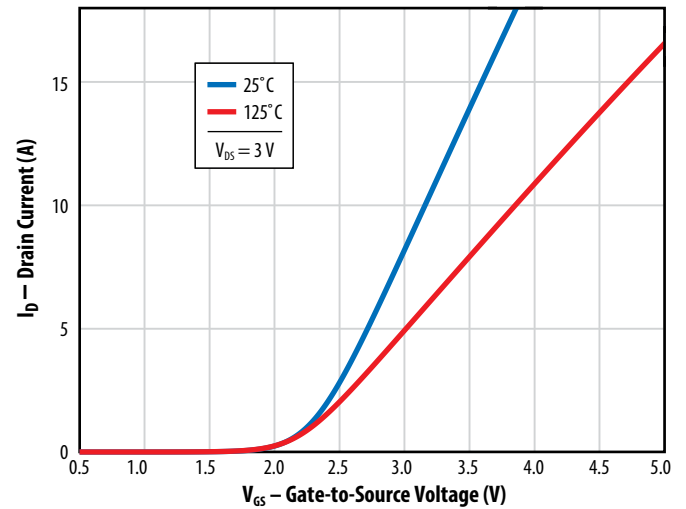
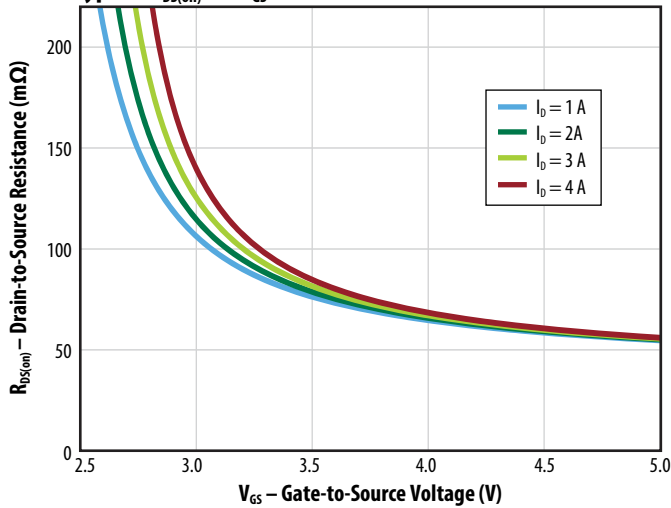
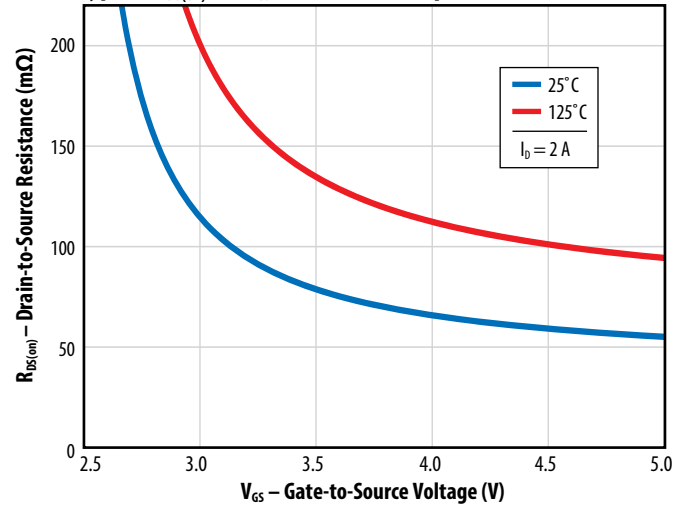
Figure 3 (Q1 & Q2):
Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4 (Q1 & Q2):
Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a (Q1): Typical Capacitance (Linear Scale)

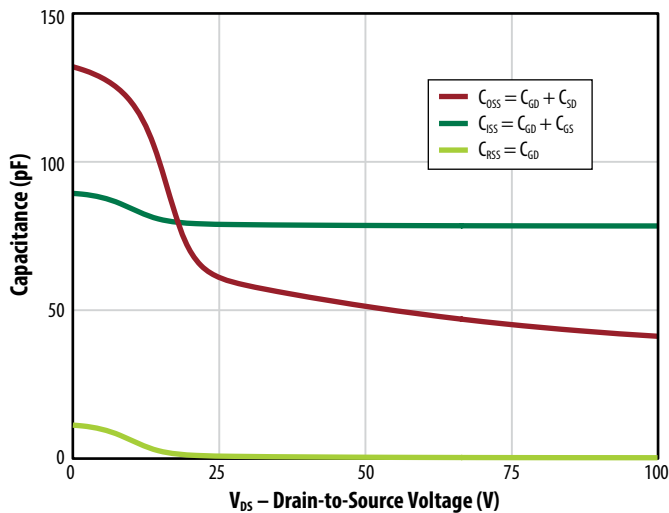


Figure 5b (Q1): Typical Capacitance (Log Scale)

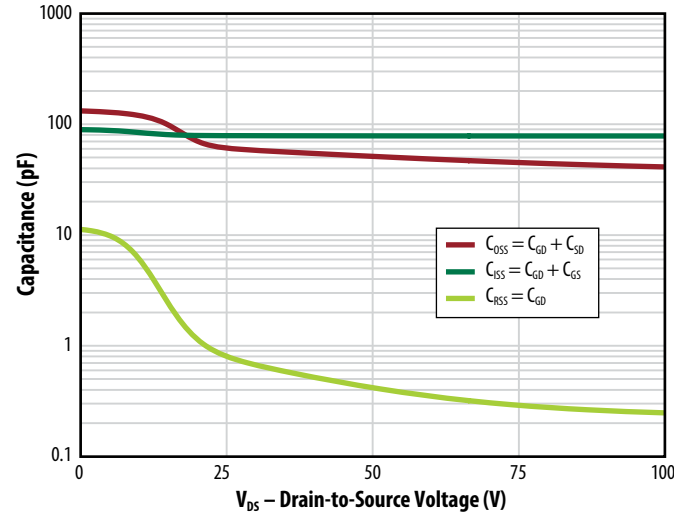


Figure 5c (Q2): Typical Capacitance (Linear Scale)

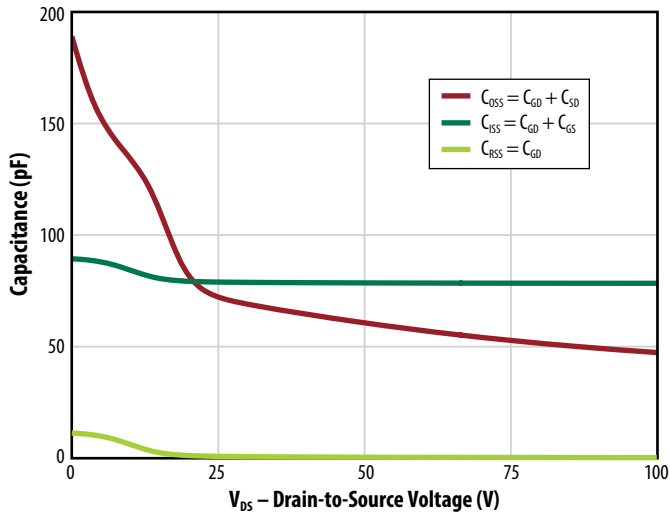


Figure 5d (Q2): Typical Capacitance (Log Scale)

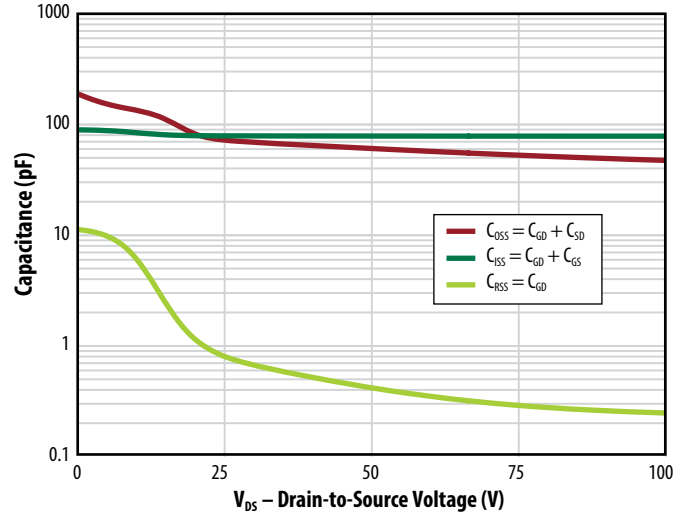
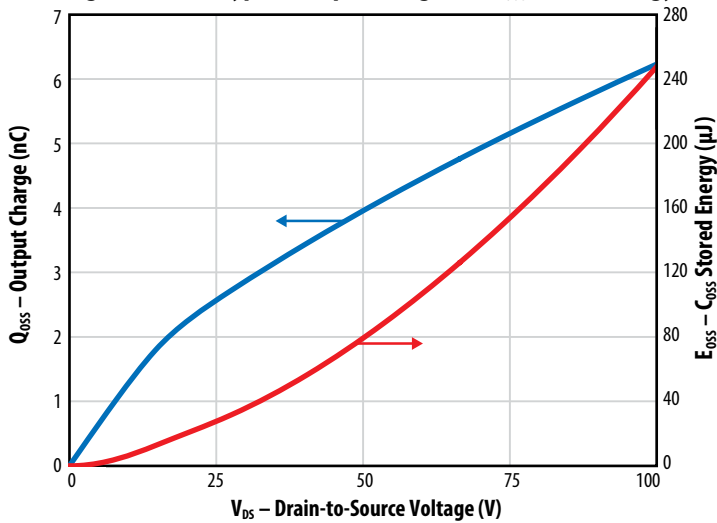
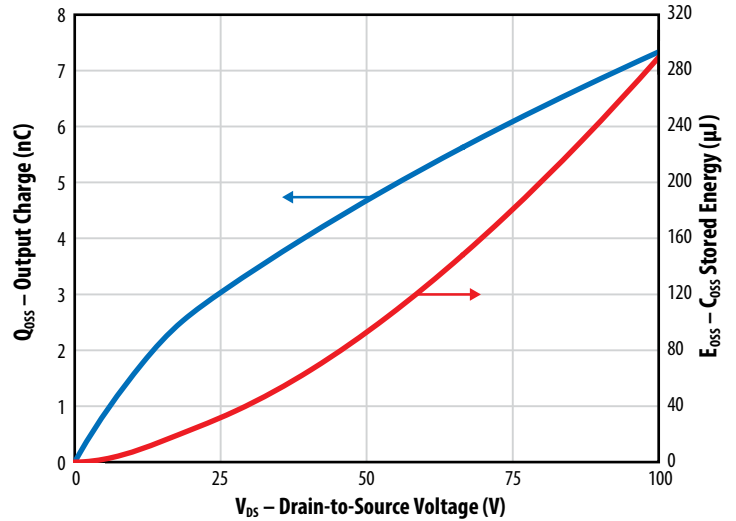
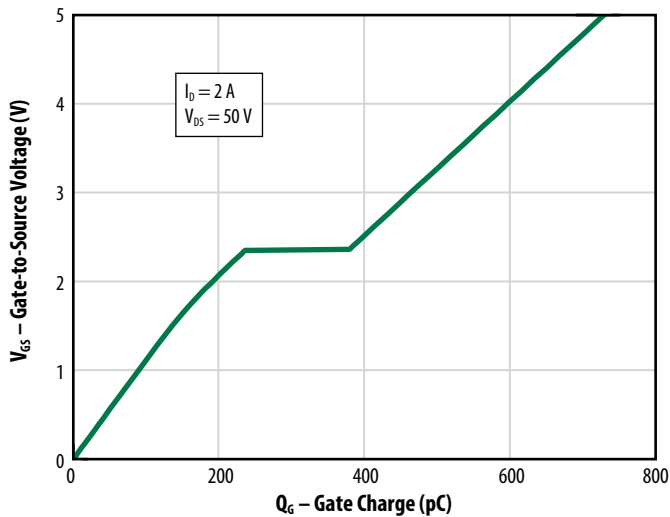
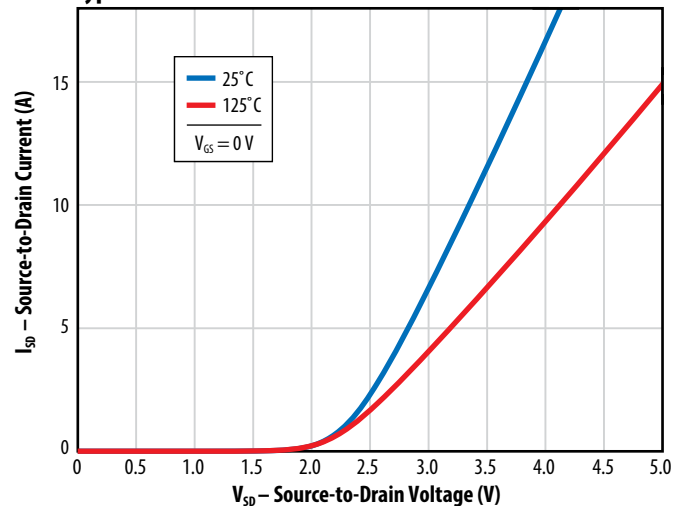
Figure 6a (Q1): Typical Output Charge and C_{oss} Stored EnergyFigure 6b (Q2): Typical Output Charge and C_{oss} Stored Energy

Figure 7 (Q1 & Q2): Typical Gate Charge

Figure 8 (Q1 & Q2):
Typical Reverse Drain-Source Characteristics

Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9 (Q1 & Q2):
Typical Normalized On-State Resistance vs. Temperature

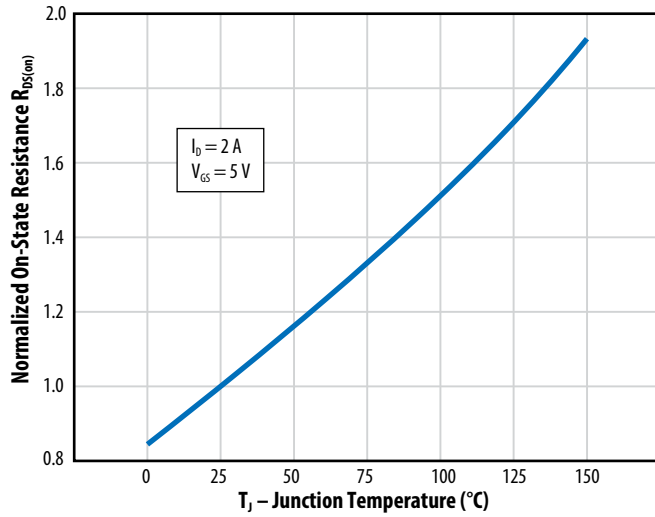


Figure 10 (Q1 & Q2):
Typical Normalized Threshold Voltage vs. Temperature

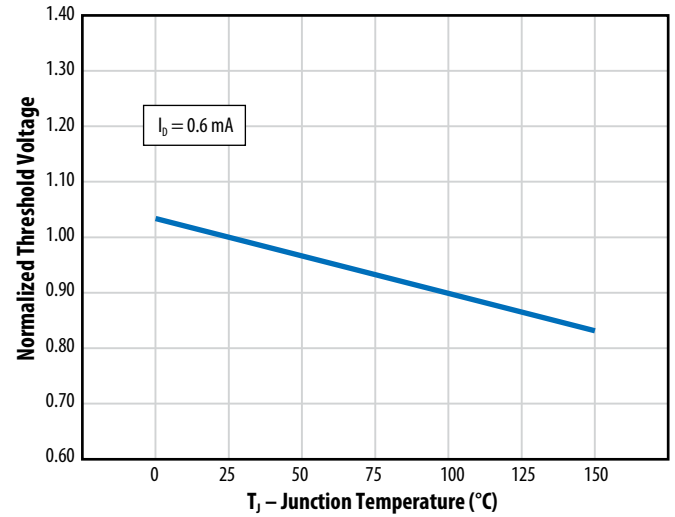


Figure 12 (Q1 & Q2): Typical Transient Thermal Response Curves

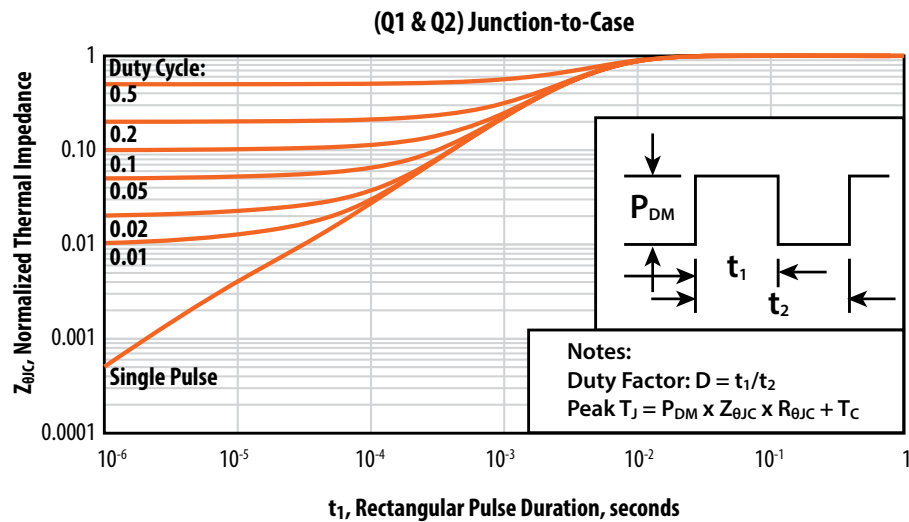
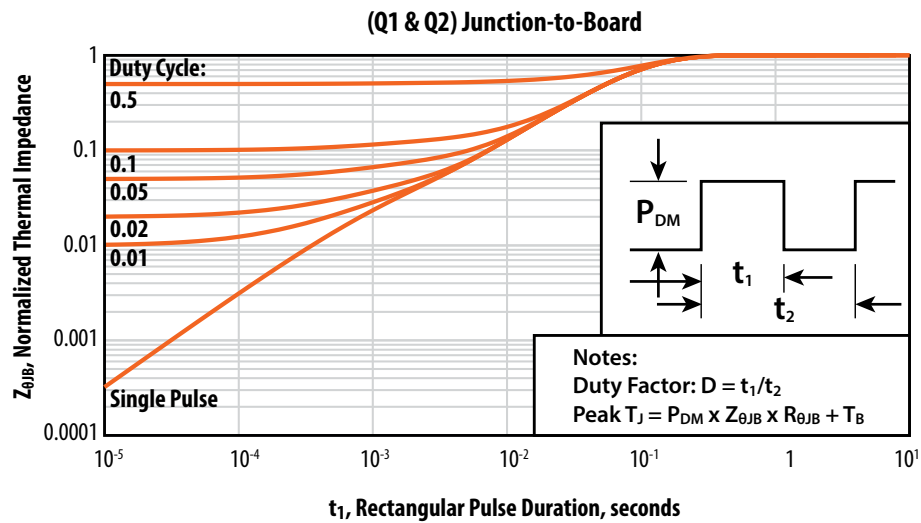
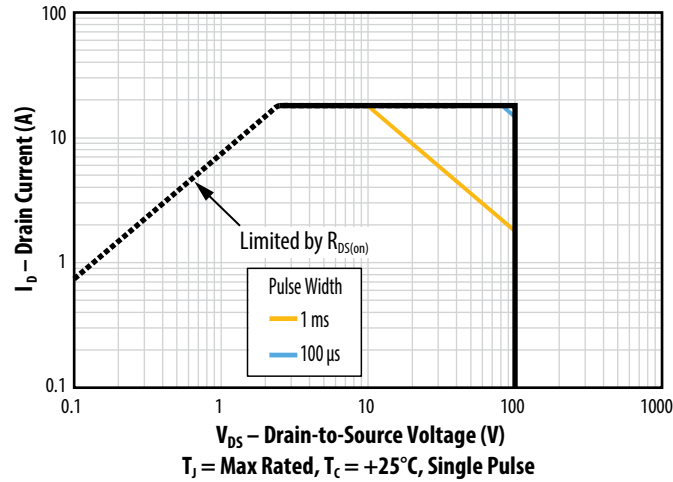
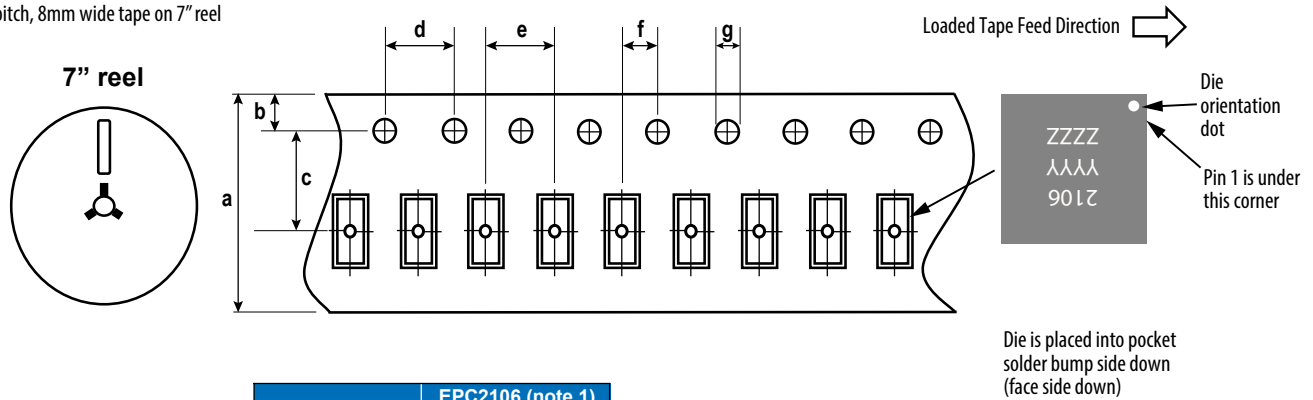


Figure 12 (Q1 & Q2): Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

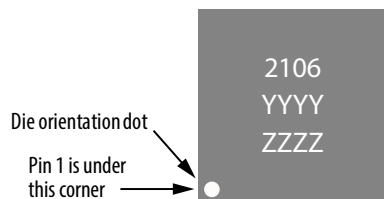


Dimension (mm)	EPC2106 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

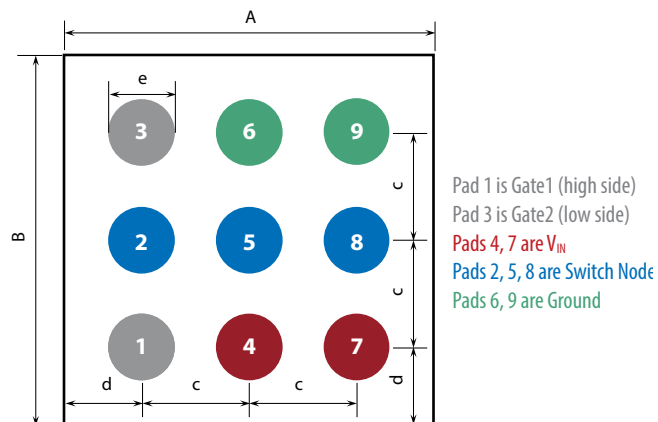
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2106	2106	YYYY	ZZZZ

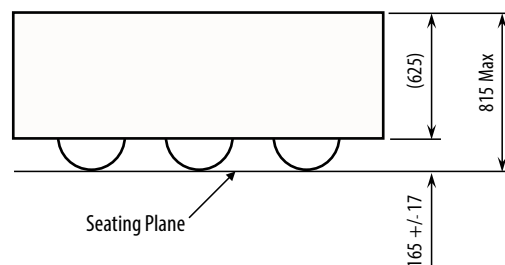
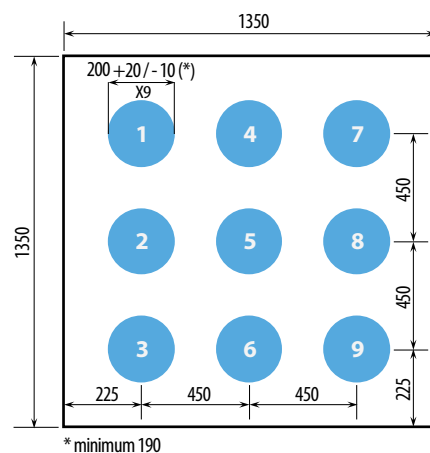
DIE OUTLINE

Solder Bump View

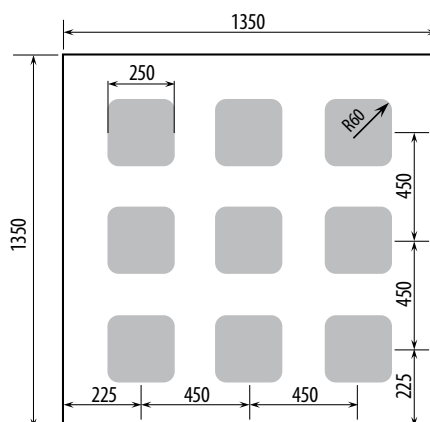


DIM	Micrometers		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
C	450	450	450
D	210	225	240
E	187	208	229

Side View

**RECOMMENDED LAND PATTERN**(measurements in μm)

The land pattern is solder mask defined.

RECOMMENDED STENCIL DRAWING(measurements in μm)Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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