

MOSFET – N-Channel, Shielded Gate POWERTRENCH[®] 40 V, 80 A, 2.1 mΩ

FDMC8360L

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 2.1 mΩ at V_{GS} = 10 V, I_D = 27 A
- Max $R_{DS(on)}$ = 3.1 mΩ at V_{GS} = 4.5 V, I_D = 22 A
- High Performance Technology for Extremely Low $R_{DS(on)}$
- Termination is Lead-Free
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Application

- DC-DC Conversion

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

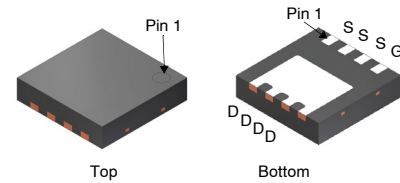
Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		A
	–Continuous T_C = 25°C	80	
	–Continuous T_A = 25°C (Note 1a)	27	
	–Pulsed (Note 4)	240	
EAS	Single Pulse Avalanche Energy (Note 3)	294	mJ
P_D	Power Dissipation T_C = 25°C	54	W
	Power Dissipation T_A = 25°C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

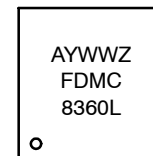
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	53	°C/W

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
40 V	2.1 mΩ @ 10 V	80 A
	3.1 mΩ @ 4.5 V	



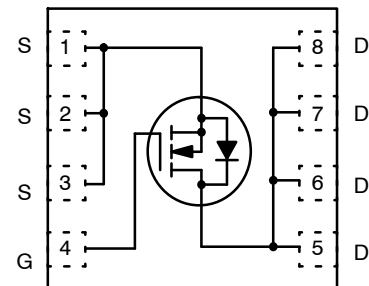
WDFN8 3.3x3.3, 0.65P
CASE 483AW

MARKING DIAGRAM



FDMC8360L = Specific Device Code
A = Assembly Site
YWW = Date Code
Z = Assembly Lot Code

PIN ASSIGNMENT



N-Channel MOSFET

ORDERING INFORMATION

Device	Package	Shipping [†]
FDMC8360L	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

ΔBV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	40	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	–	22	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	–	–6	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 27\ \text{A}$	–	1.6	2.1	m Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 22\ \text{A}$	–	2.3	3.1	
		$V_{GS} = 10\ \text{V}$, $I_D = 27\ \text{A}$, $T_J = 125^\circ\text{C}$	–	2.2	2.9	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 27\ \text{A}$	–	138	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	4140	5795	pF
C_{oss}	Output Capacitance		–	1230	1725	pF
C_{rss}	Reverse Transfer Capacitance		–	36	60	pF
R_g	Gate Resistance		0.1	0.9	2.7	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 20 V, I _D = 27 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		–	15	28	ns
t _r	Rise Time			–	6.7	14	ns
t _{d(off)}	Turn-Off Delay Time			–	38	60	ns
t _f	Fall Time			–	5.3	11	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V	V _{DD} = 20 V I _D = 27 A	–	57	80	nC
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 4.5 V		–	26	37	nC
Q _{gs}	Gate to Source Charge			–	11	–	nC
Q _{gd}	Gate to Drain “Miller” Charge			–	5.7	–	nC

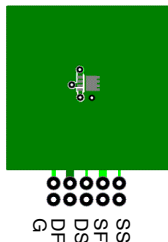
DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 27\ \text{A}$ (Note 2)	–	0.8	1.3	V
		$V_{GS} = 0\ \text{V}$, $I_S = 1.9\ \text{A}$ (Note 2)	–	0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 27\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	49	80	ns
Q_{rr}	Reverse Recovery Charge		–	29	46	nC

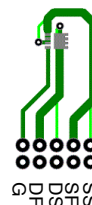
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. 125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.
- E_{AS} of 294 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\ \text{mH}$, $I_{AS} = 14\ \text{A}$, $V_{DD} = 40\ \text{V}$, $V_{GS} = 10\ \text{V}$. 100% test at $L = 0.1\ \text{mH}$, $I_{AS} = 44\ \text{A}$.
- Pulsed I_d limited by junction temperature, $t_d \leq 100\ \mu\text{s}$, please refer to SOA curve for more details.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

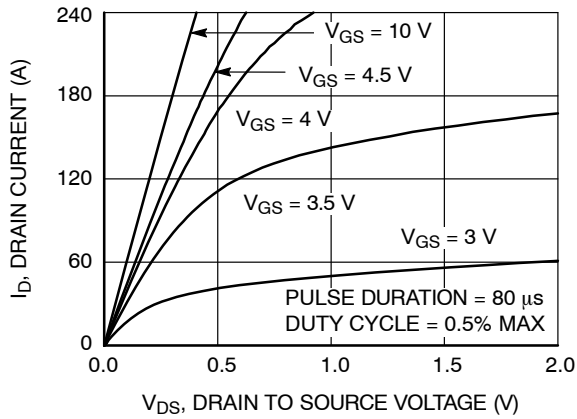


Figure 1. On-Region Characteristics

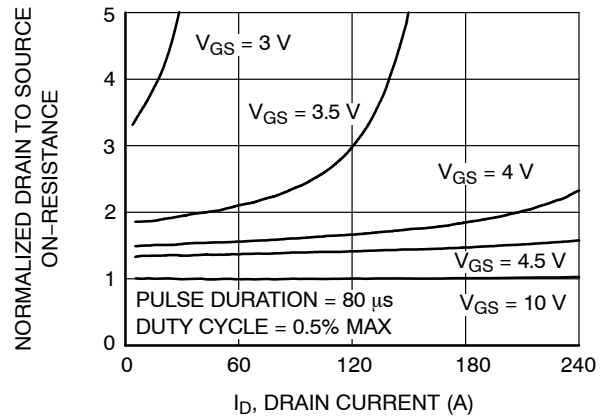


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

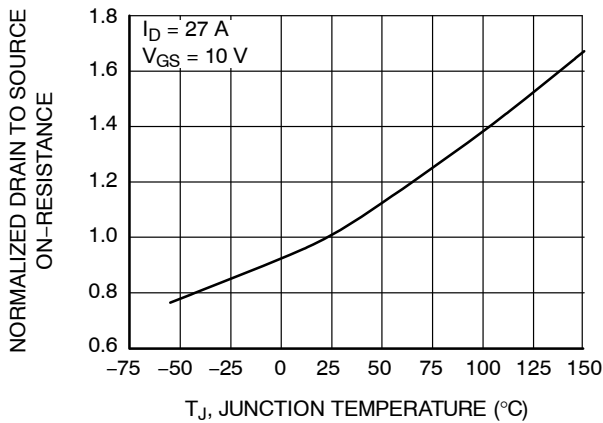


Figure 3. Normalized On Resistance vs. Junction Temperature

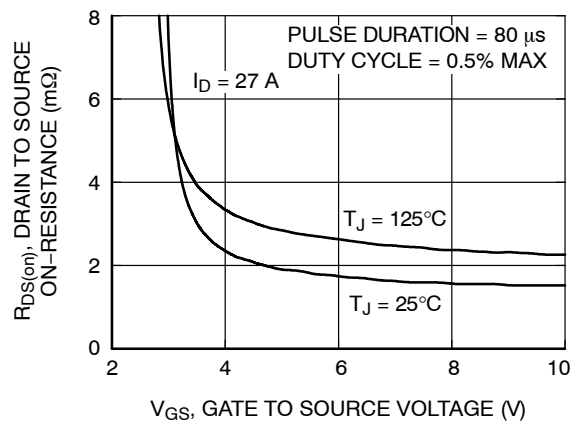


Figure 4. On-Resistance vs. Gate to Source Voltage

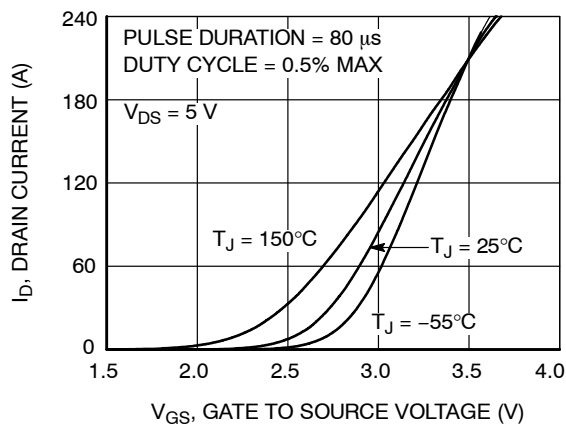


Figure 5. Transfer Characteristics

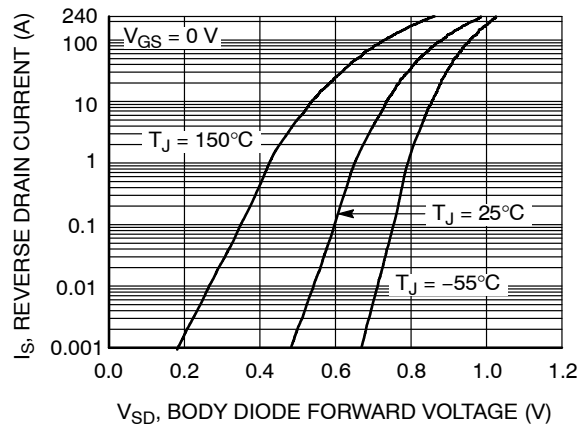


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

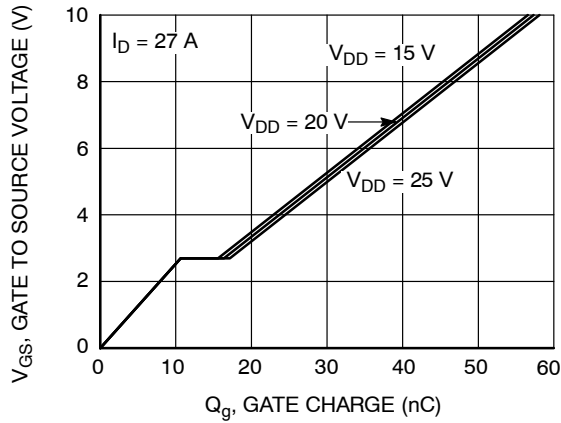


Figure 7. Gate Charge Characteristics

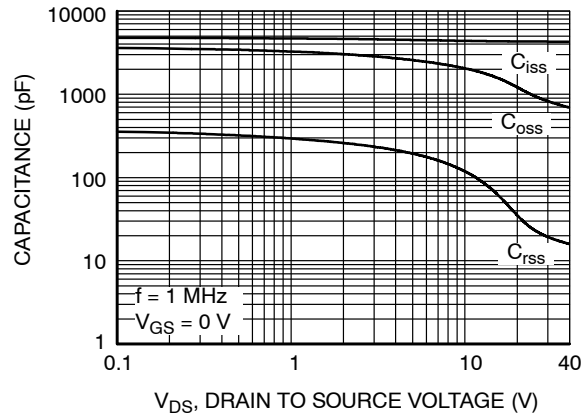


Figure 8. Capacitance vs. Drain to Source Voltage

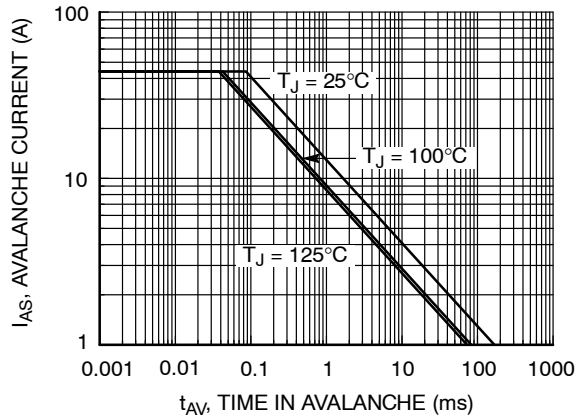


Figure 9. Unclamped Inductive Switching Capability

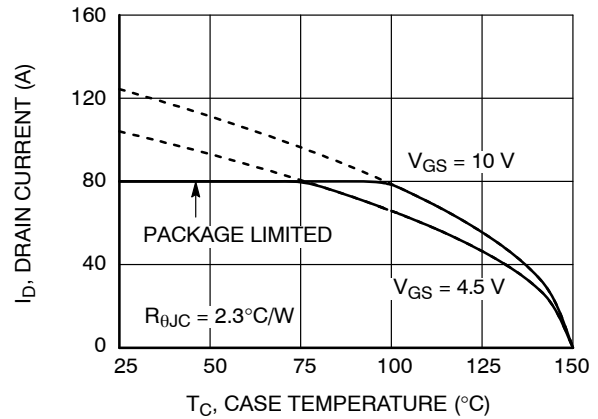


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

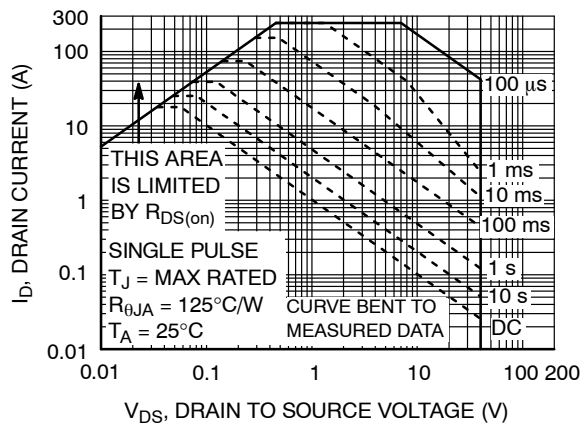


Figure 11. Forward Bias Safe Operating Area

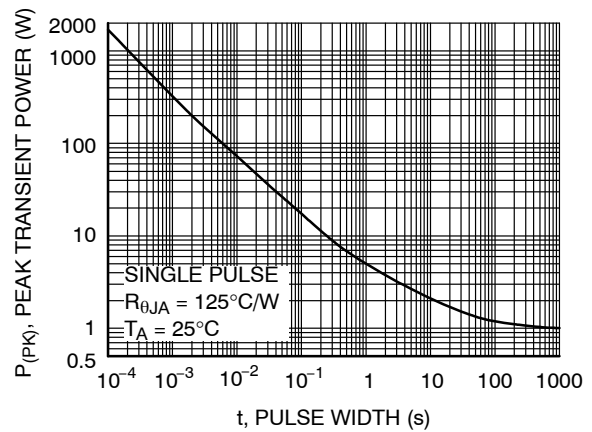


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

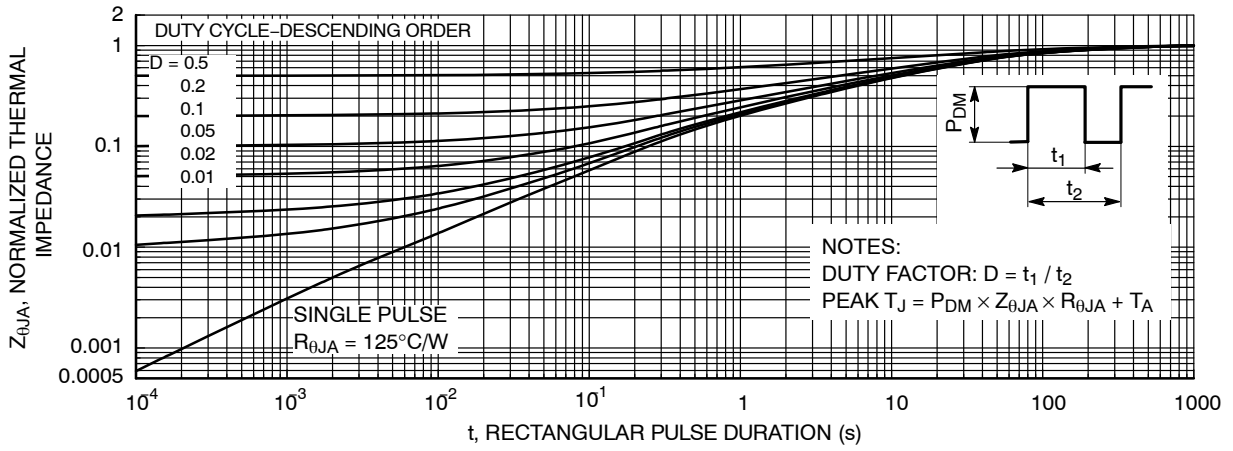
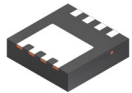
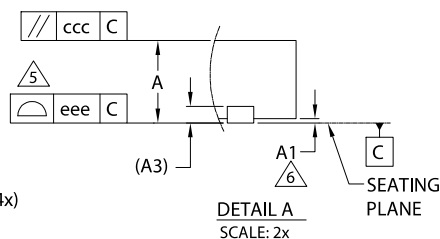
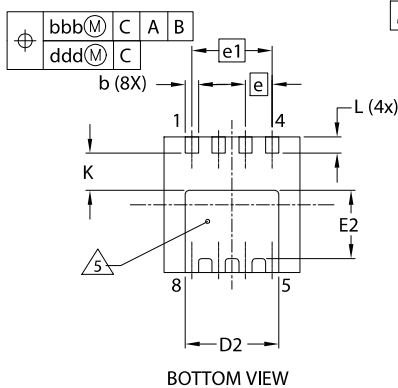
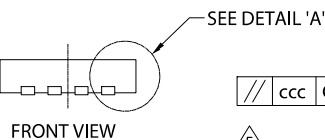
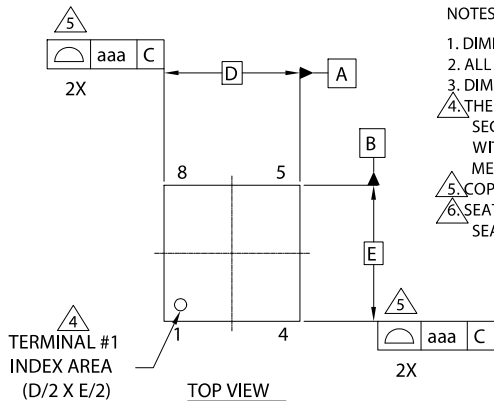


Figure 13. Junction-to-Ambient Transient Thermal Response Curve


WDFN-8 3.30x3.30x0.75, 0.65P
CASE 483AW
ISSUE C

DATE 25 SEP 2026

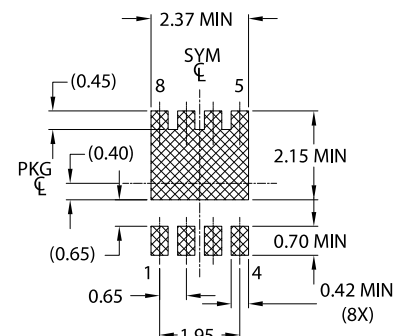


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	—	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.30 BSC		
D2	2.17	2.27	2.37
E	3.30 BSC		
E2	1.56	1.66	1.76
e	0.65 BSC		
e1	1.95 BSC		
K	0.90	—	—
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

GENERIC MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.


RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERM/D.

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DESCRIPTION:	WDFN-8 3.30x3.30x0.75, 0.65P	PAGE 1 OF 1

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