

FDS6681Z-VB Datasheet

P-Channel 30 V (D-S) MOSFET

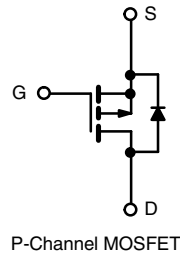
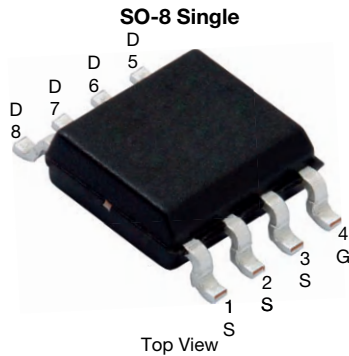
PRODUCT SUMMARY	
V_{DS} (V)	-30
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0050
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0080
Q_g typ. (nC)	27
I_D (A)	18
Configuration	Single

FEATURES

- Trench Gen IV p-channel power MOSFET
- Enables higher power density
- 100 % R_g and UIS tested



RoHS
COMPLIANT
HALOGEN
FREE



APPLICATIONS

- Battery management in mobile devices
- Adapter and charger switch
- Battery switch
- Load switch

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-30	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	-18	A
	$T_C = 70$ °C		-13	
	$T_A = 25$ °C		-11	
	$T_A = 70$ °C		-8	
Pulsed drain current ($t = 100$ μ s)		I_{DM}	-145	
Continuous source-drain diode current	$T_C = 25$ °C	I_S	-5	
	$T_A = 25$ °C		-2.8 ^{b, c}	
Single pulse avalanche current	$L = 0.1$ mH	I_{AS}	-25	mJ
Single pulse avalanche energy		E_{AS}	31.2	
Maximum power dissipation	$T_C = 25$ °C	I_P	5.6	W
	$T_C = 70$ °C		3.6	
	$T_A = 25$ °C		3.1 ^{b, c}	
	$T_A = 70$ °C		2 ^{b, c}	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	$t \leq 10$ s	R_{thJA}	34	40	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJF}	18	22	

Notes

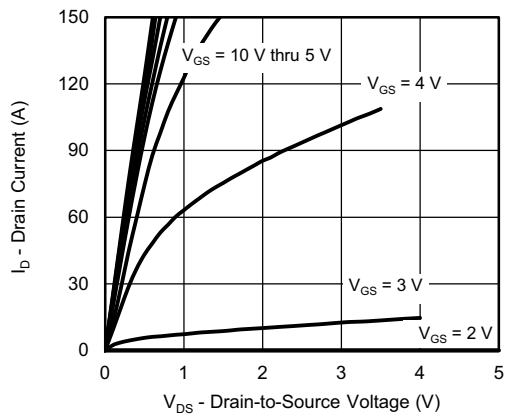
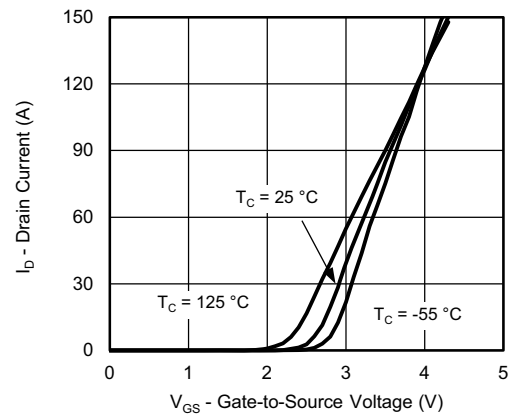
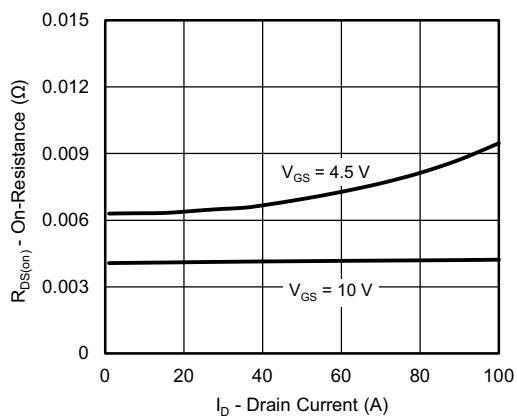
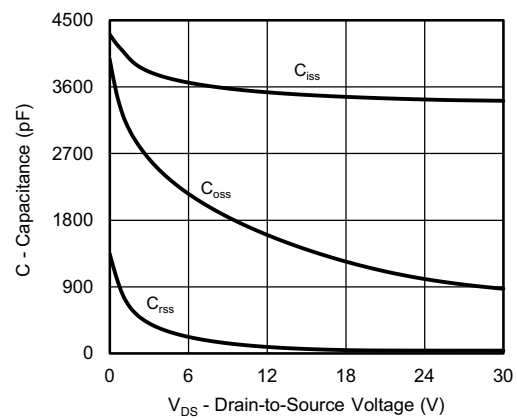
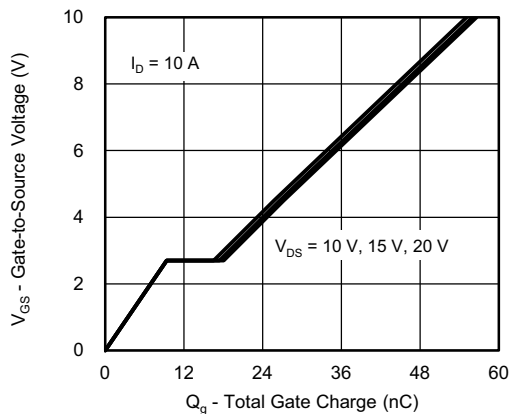
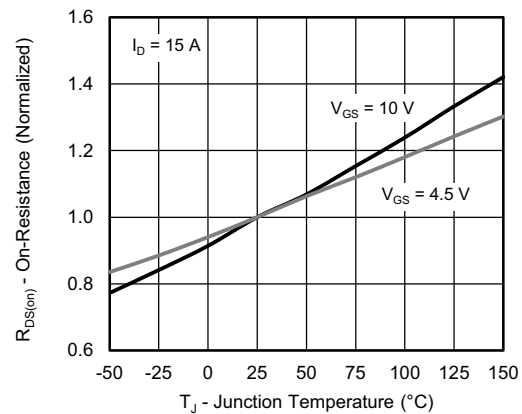
- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- The SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 85 °C/W
- $T_C = 25$ °C

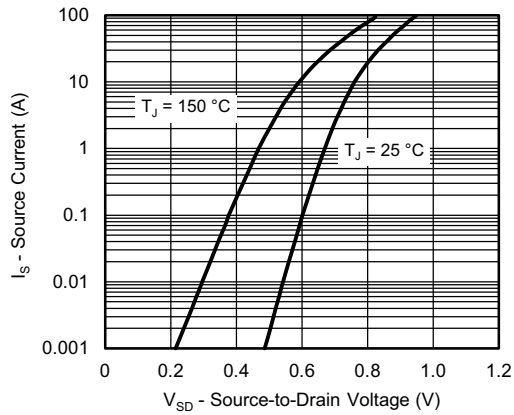
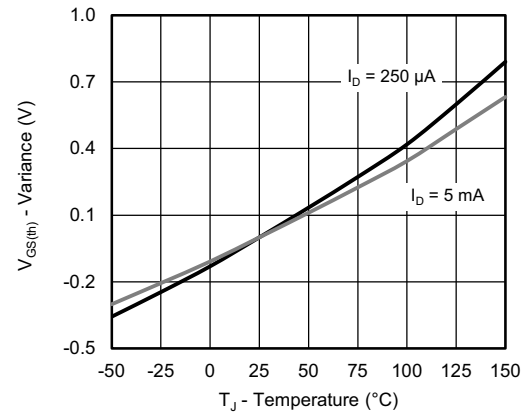
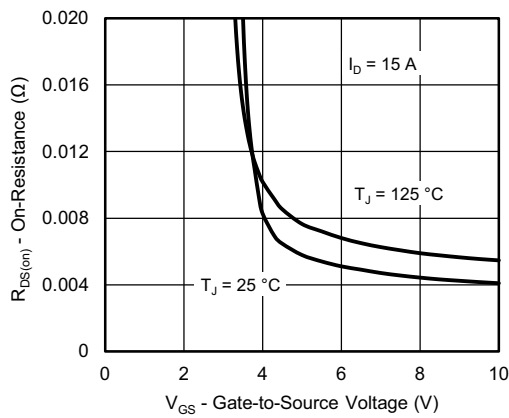
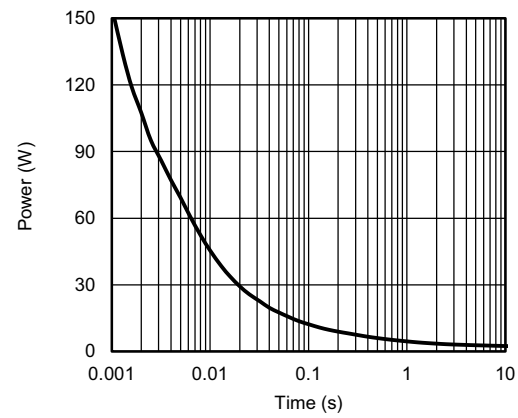
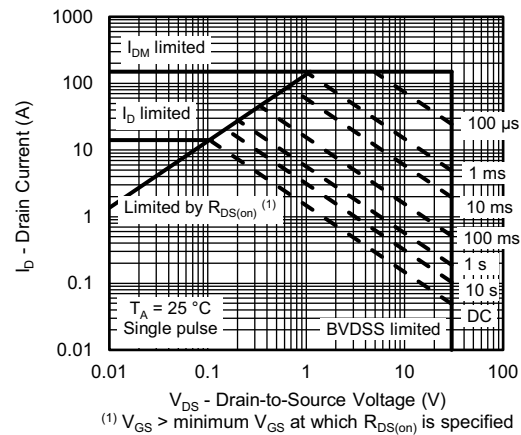
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-30	-	-	V	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -10 mA	-	-17	-	mV/°C	
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = -250 μA	-	5.5	-		
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	-1	-	-2.2	V	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +16 / -20 V	-	-	100	nA	
Zero gate voltage drain current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V	-	-	-1	μA	
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 70 °C	-	-	-15		
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ -10 V, V _{GS} = -10 V	-40	-	-	A	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -15 A	-	0.0050	-	Ω	
		V _{GS} = -4.5 V, I _D = -10 A	-	0.0080	-		
Forward transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -15 A	-	81	-	S	
Dynamic ^b							
Input capacitance	C _{iss}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	-	3490	-	pF	
Output capacitance	C _{oss}		-	1420	-		
Reverse transfer capacitance	C _{rss}		-	70	-		
Total gate charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -10 A	-	56	84	nC	
		V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -10 A	-	27	41		
Gate-source charge	Q _{gs}		-	9.4	-		
Gate-drain charge	Q _{gd}		-	8.2	-		
Gate resistance	R _g	f = 1 MHz	1.5	3.5	6	Ω	
Turn-on delay time	t _{d(on)}	V _{DD} = -15 V, R _L = 1.5 Ω, I _D ≅ -10 A, V _{GEN} = -10 V, R _g = 1 Ω	-	15	30	ns	
Rise time	t _r		-	6	12		
Turn-off delay time	t _{d(off)}		-	39	78		
Fall time	t _f		-	10	20		
Turn-on delay time	t _{d(on)}	V _{DD} = -15 V, R _L = 1.5 Ω, I _D ≅ -10 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	34	68		
Rise time	t _r		-	86	172		
Turn-off delay time	t _{d(off)}		-	31	62		
Fall time	t _f		-	22	44		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-5	A	
Pulse diode forward current	I _{SM}		-	-	-150		
Body diode voltage	V _{SD}	I _S = -5 A, V _{GS} = 0 V	-	-0.73	-1.1	V	
Body diode reverse recovery time	t _{rr}	I _F = -10 A, di/dt = 100 A/μs, T _J = 25 °C	-	44	88	ns	
Body diode reverse recovery charge	Q _{rr}		-	41	82	nC	
Reverse recovery fall time	t _a		-	19	-	ns	
Reverse recovery rise time	t _b		-	25	-		

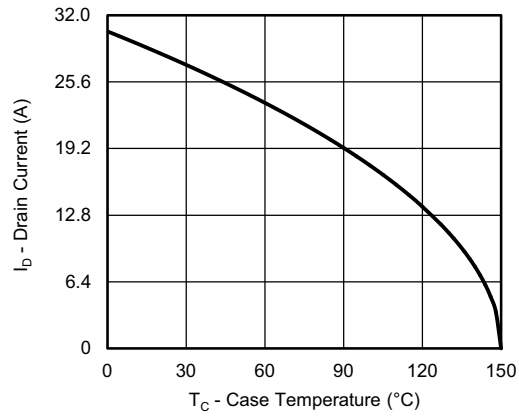
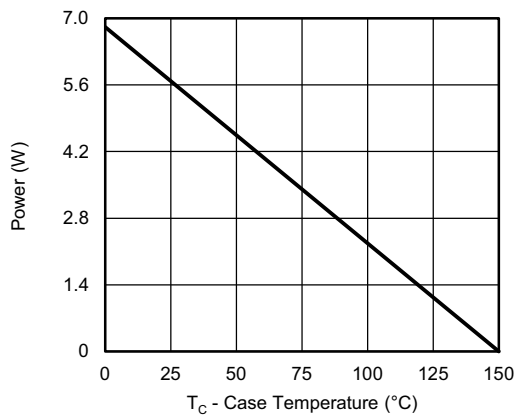
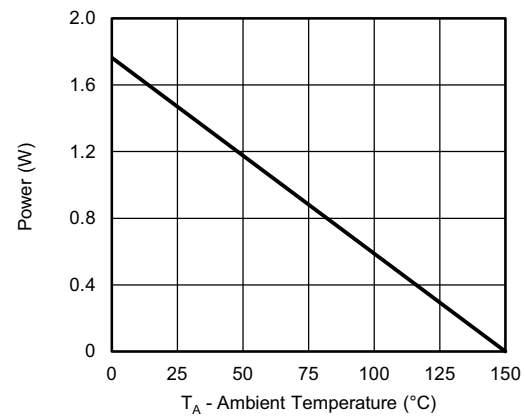
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 b. Guaranteed by design, not subject to production testing

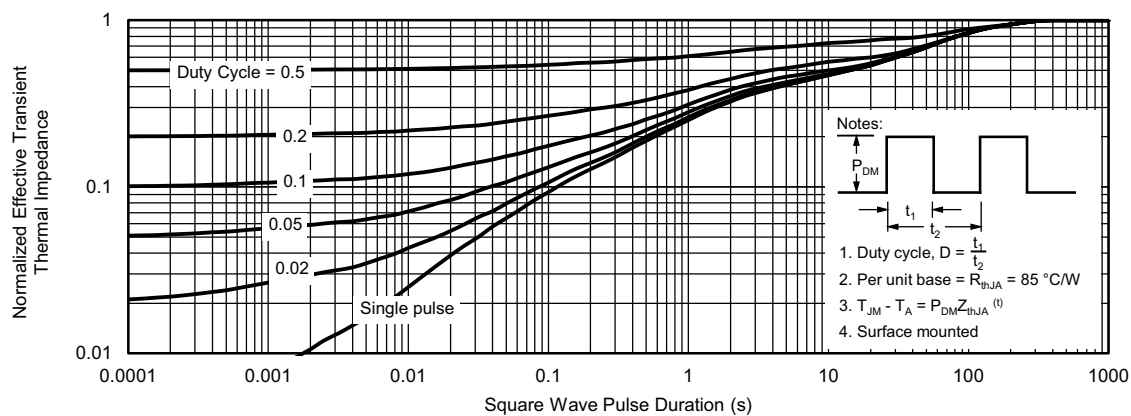
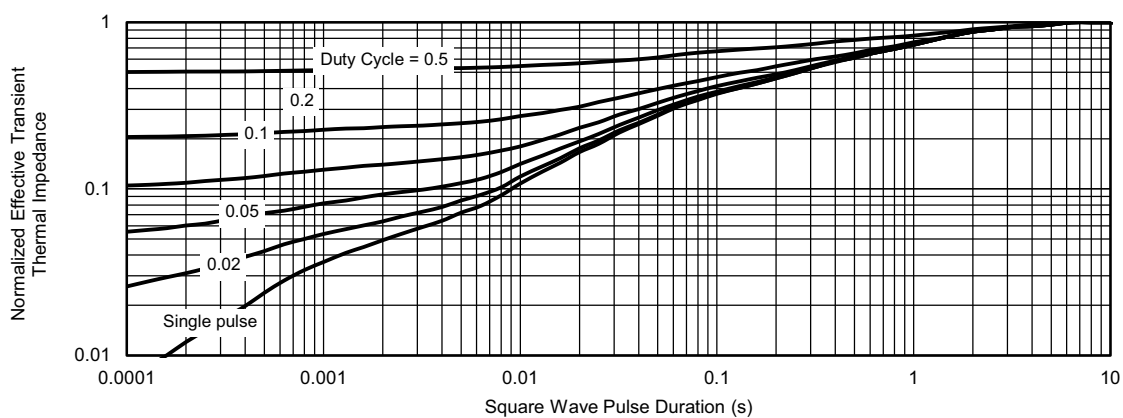
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

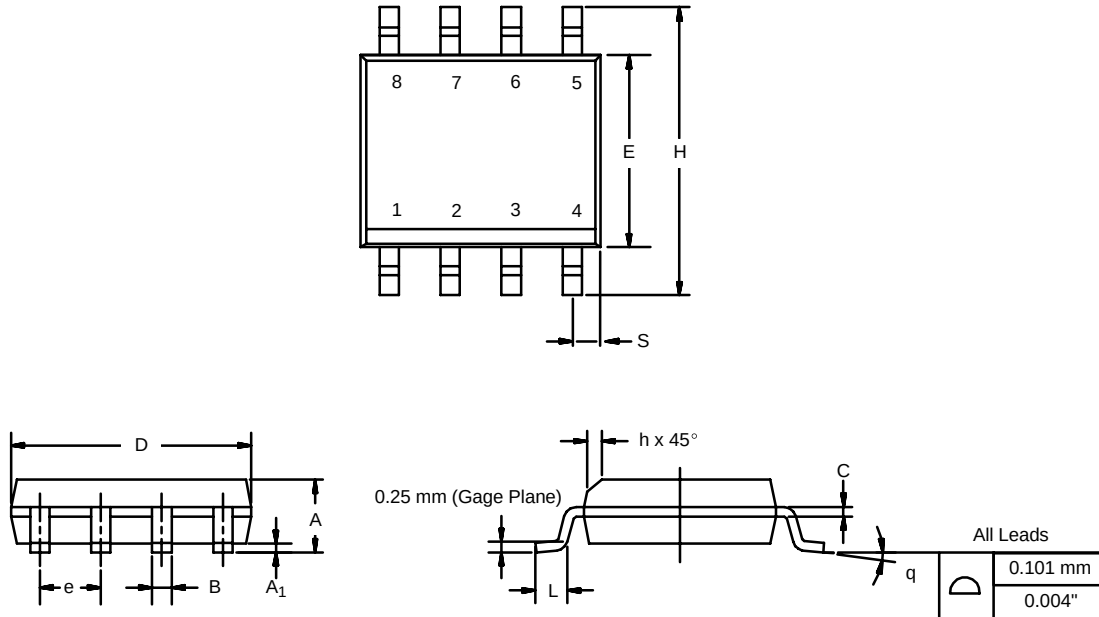
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

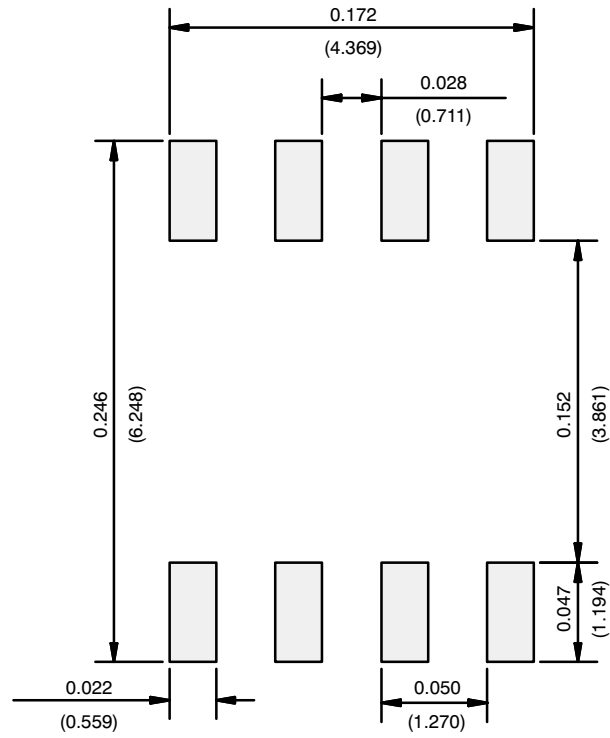
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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