

MOSFET – N-Channel, QFET[®]

1000 V, 1.6 A, 9 Ω

FQU2N100, FQD2N100

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

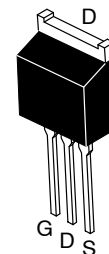
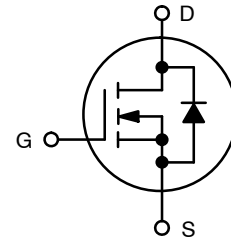
- 1.6 A, 1000 V, $R_{DS(on)} = 9\ \Omega$ (Max.) @ $V_{GS} = 10\text{ V}$, $I_D = 0.8\text{ A}$
- Low Gate Charge (Typ. 12 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25\ ^\circ\text{C}$ unless otherwise noted)

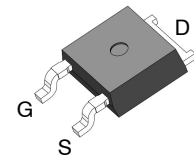
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	1000	V
Drain Current – Continuous ($T_C = 25\ ^\circ\text{C}$) – Continuous ($T_C = 100\ ^\circ\text{C}$)	I_D	1.6 1.0	A
Drain Current – Pulsed (Note 2)	I_{DM}	6.4	A
Gate-Source Voltage	V_{GSS}	± 30	V
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	160	mJ
Avalanche Current (Note 2)	I_{AR}	1.6	A
Repetitive Avalanche Energy (Note 2)	E_{AR}	5.0	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	5.5	V/ns
Power Dissipation ($T_A = 25\ ^\circ\text{C}$) *	P_D	2.5	W
Power Dissipation ($T_C = 25\ ^\circ\text{C}$) – Derate above $25\ ^\circ\text{C}$		50 0.4	W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to $+150$	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes, 1/8" (from case for 5 seconds)	T_L	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
1000 V	$9\ \Omega @ 10\text{ V}$	1.6 A

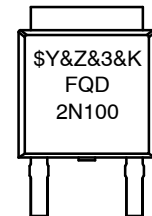
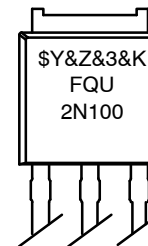


DPAK3 (IPAK)
CASE 369AR



DPAK3 (TO-252 3 LD)
CASE 369AS

MARKING DIAGRAMS



FQU2N100,
FQD2N100 = Device Code
\$Y = onsemi Logo
&Z = Assembly Location
&3 = 3-Digit Date Code
&K = 2-Digits Lot Run Traceability Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FQD2N100TM	DPAK3 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 1)

FQU2N100TU	DPAK3 (IPAK) (Pb-Free)	70 Units / Tube
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[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

1. **DISCONTINUED:** This device is not available. Please contact your onsemi representative for information. The most current information on this device may be available on [www.onsemi.com](#).

FQU2N100, FQD2N100

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (minimum pad of 2 oz copper) , Max.	110	$^{\circ}\text{C}/\text{W}$
	Thermal Resistance, Junction-to-Ambient (* 1 in2 pad of 2 oz copper), Max.	50	

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	1000	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	0.97 6	–	$\text{V}/^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 1000\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	10	μA
		$V_{DS} = 800\ \text{V}$, $T_C = 125^{\circ}\text{C}$	–	–	100	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	-100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain-Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 0.8\ \text{A}$	–	7.1	9	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\ \text{V}$, $I_D = 0.8\ \text{A}$	–	1.9	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1.0\ \text{MHz}$	–	400	520	pF
C_{oss}	Output Capacitance		–	40	52	
C_{rss}	Reverse Transfer Capacitance		–	5	6.5	

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 500\ \text{V}$, $I_D = 2.0\ \text{A}$, $R_G = 25\ \Omega$ (Note 5)	–	13	35	ns
t_r	Turn-On Rise Time		–	30	70	
$t_{d(off)}$	Turn-Off Delay Time		–	25	60	
t_f	Turn-Off Fall Time		–	35	80	
Q_g	Total Gate Charge	$V_{DS} = 800\ \text{V}$, $I_D = 2.0\ \text{A}$, $V_{GS} = 10\ \text{V}$ (Note 5)	–	12	15.5	nC
Q_{gs}	Gate-Source Charge		–	2.5	–	
Q_{gd}	Gate-Drain Charge		–	6.5	–	

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current		–	–	1.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		–	–	6.0	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 1.6\ \text{A}$	–	–	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ \text{V}$, $I_S = 2.0\ \text{A}$, $di_F/dt = 100\ \text{A}/\mu\text{s}$	–	520	–	ns
Q_{rr}	Reverse Recovery Charge		–	2.3	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L = 120\ \text{mH}$, $I_{AS} = 1.6\ \text{A}$, $V_{DD} = 50\ \text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 2.0\ \text{A}$, $di/dt \leq 300\ \text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$.

5. Essentially independent of operating temperature.



TYPICAL CHARACTERISTICS

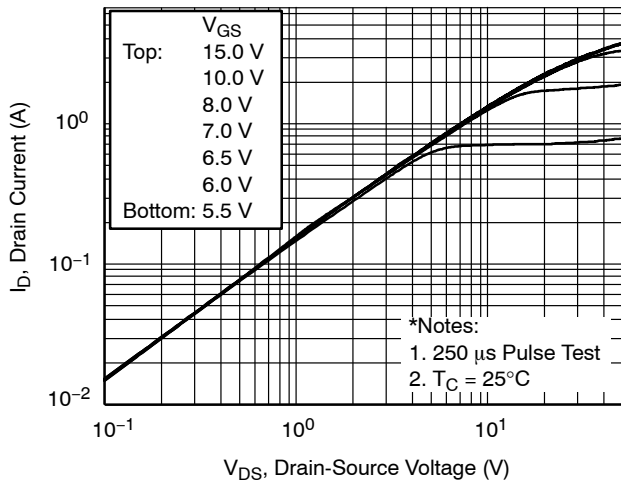


Figure 1. On-Region Characteristics

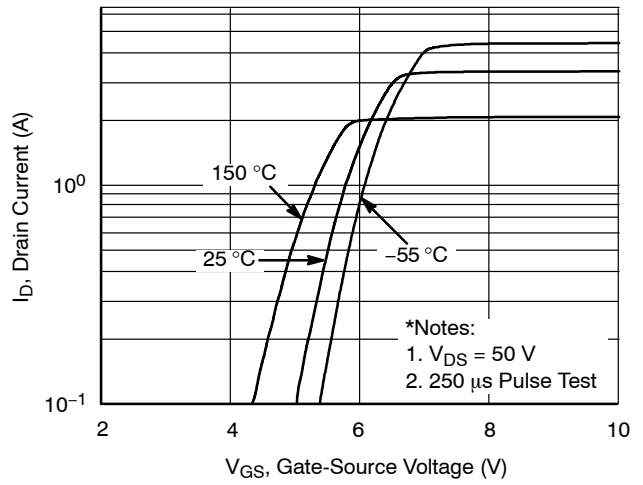


Figure 2. Transfer Characteristics

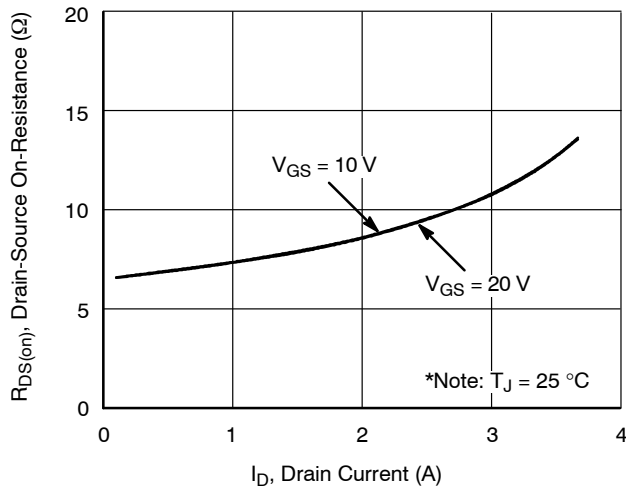


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

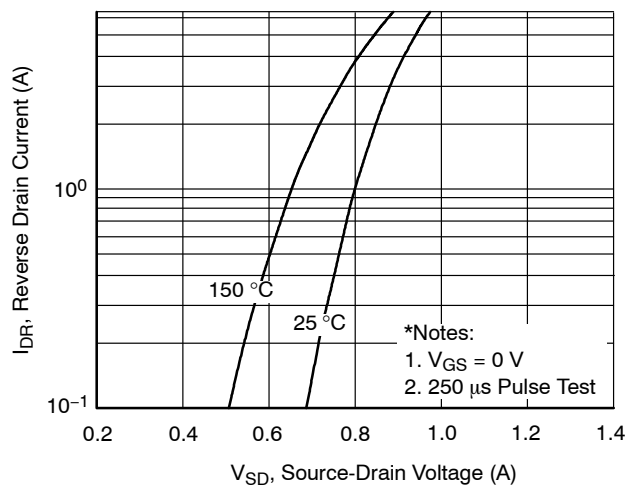


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

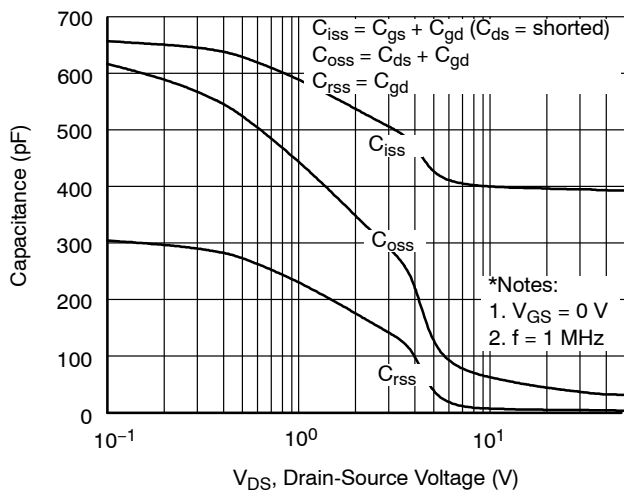


Figure 5. Capacitance Characteristics

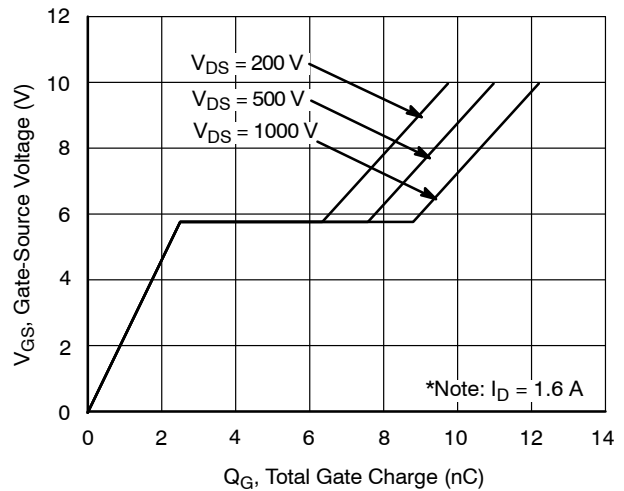
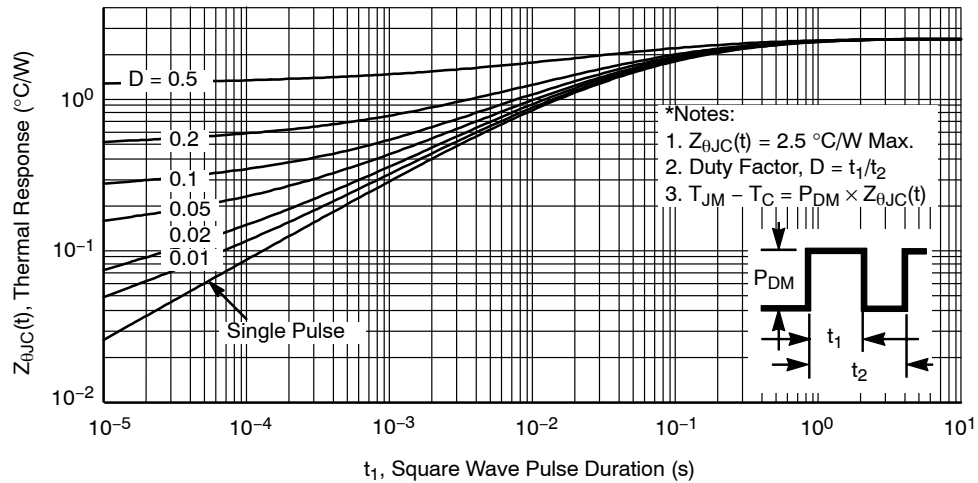
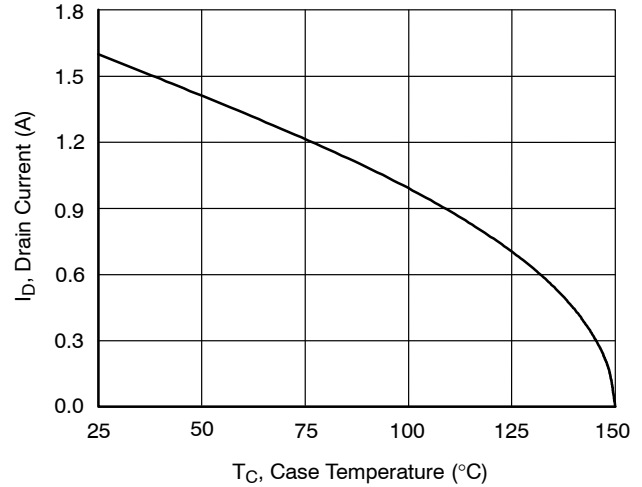
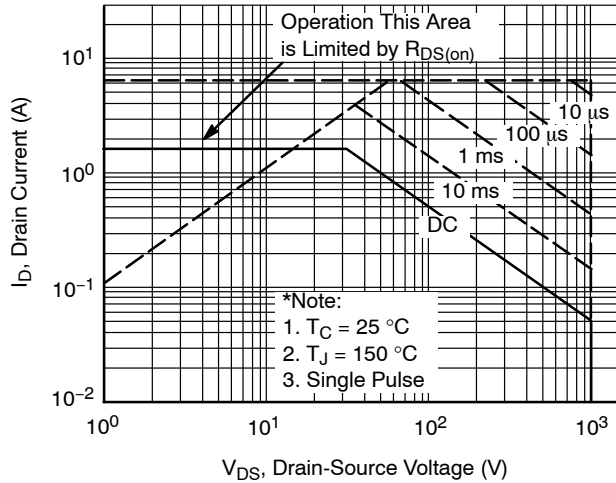
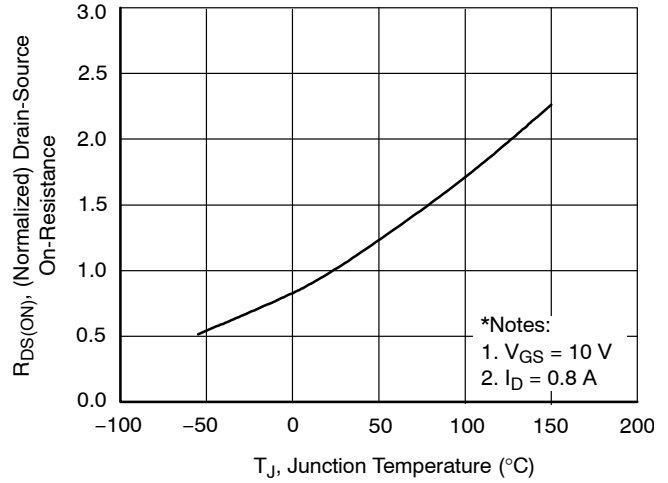
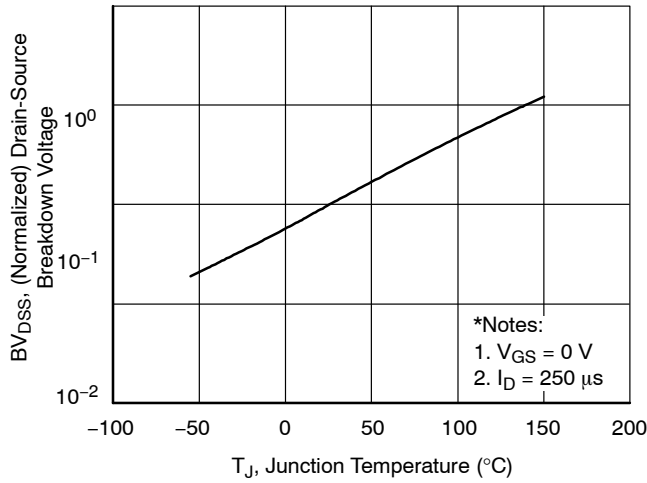


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)



FQU2N100, FQD2N100

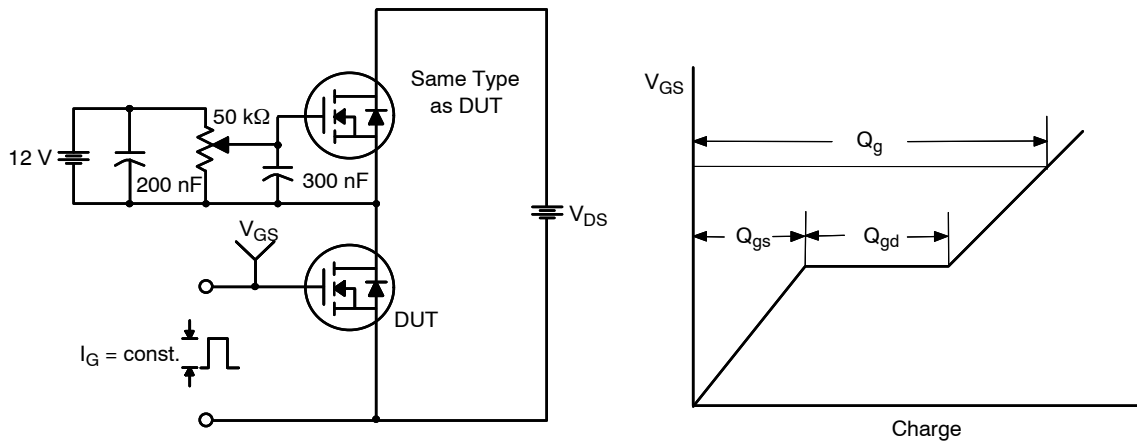


Figure 12. Gate Charge Test Circuit & Waveform

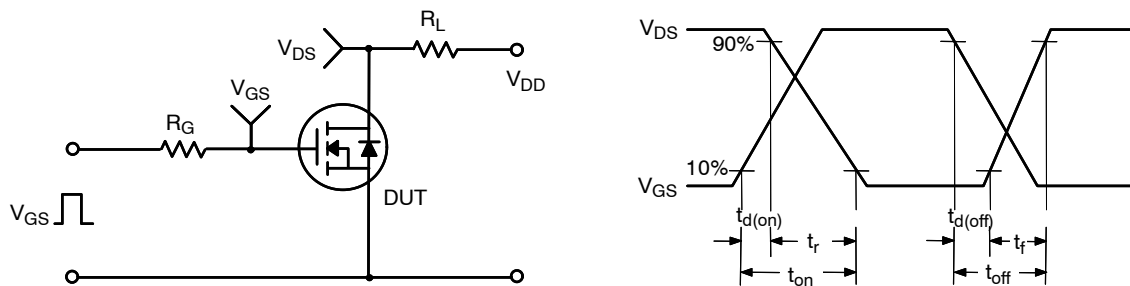


Figure 13. Resistive Switching Test Circuit & Waveforms

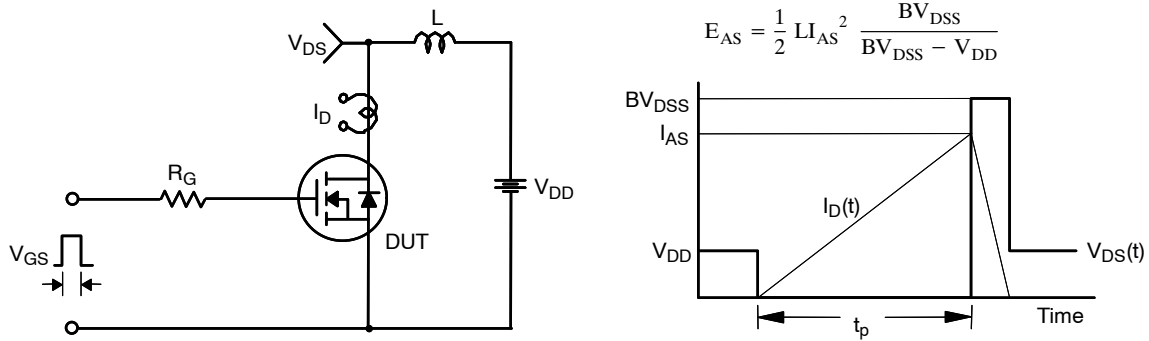


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FQU2N100, FQD2N100

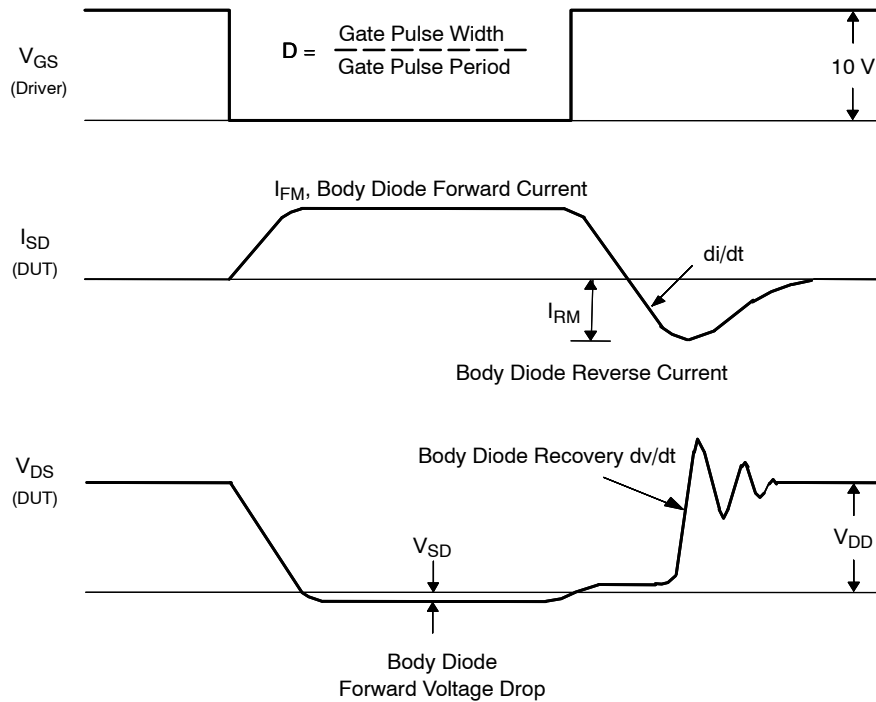
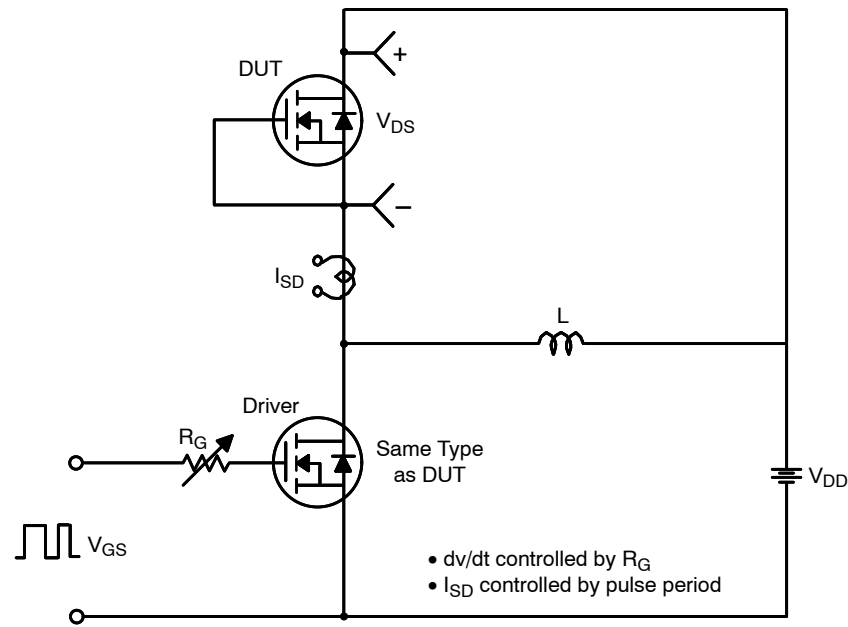


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

FQU2N100, FQD2N100

REVISION HISTORY

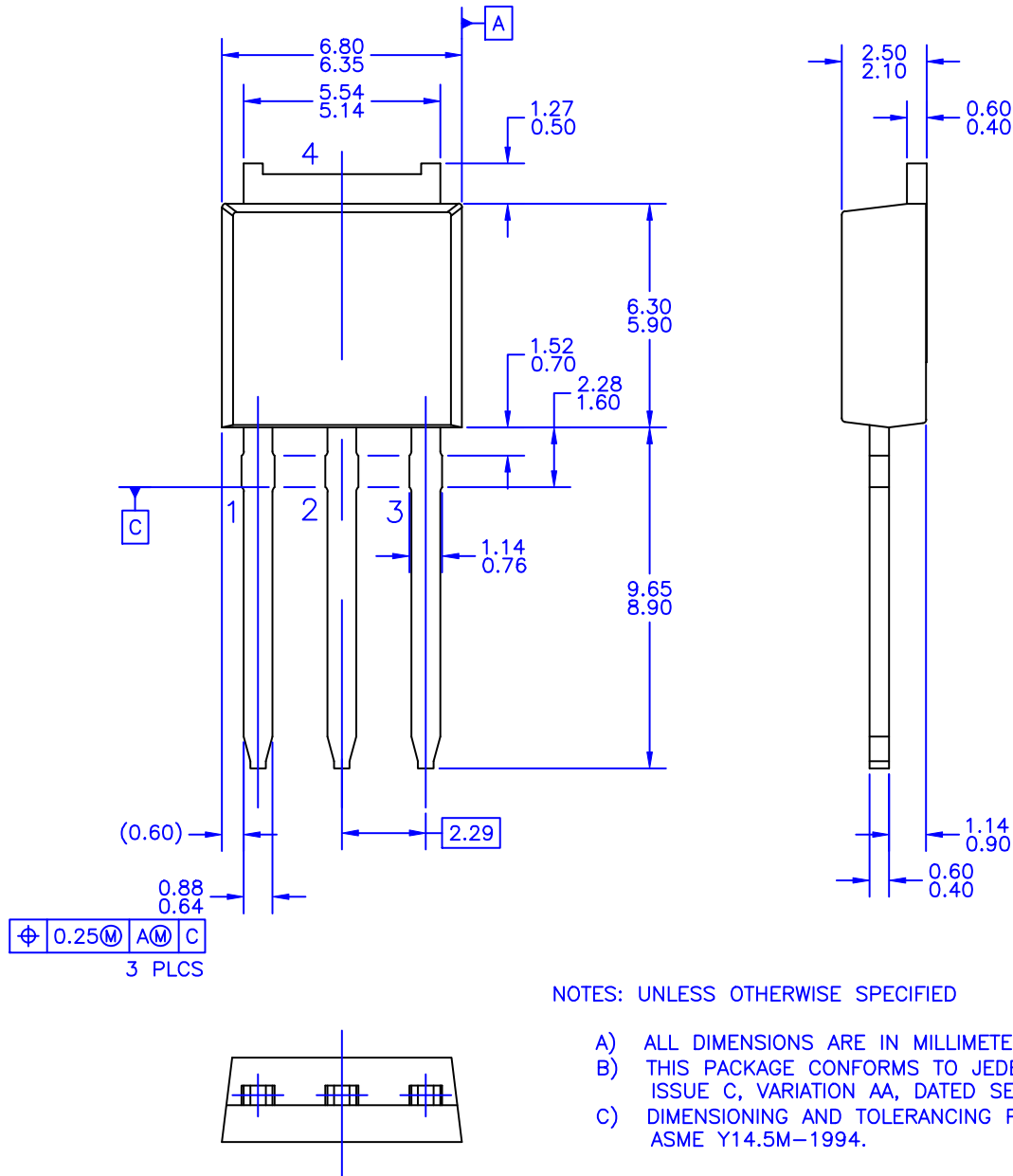
Revision	Description of Changes	Date
5	Added G, D, S description on the 1 st page images (packages) and marked discontinued part number.	10/1/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



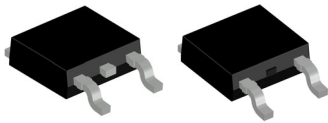
DPAK3 (IPAK)
CASE 369AR
ISSUE O

DATE 30 SEP 2016

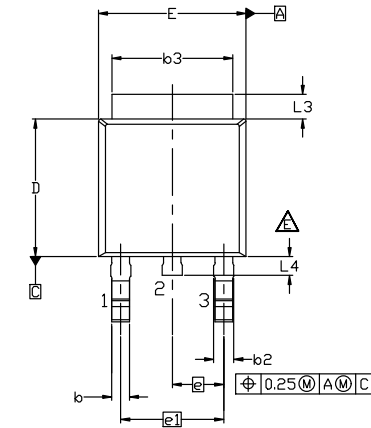


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DESCRIPTION:	DPAK3 (IPAK)	PAGE 1 OF 1

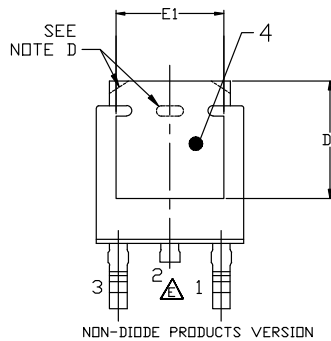
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DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

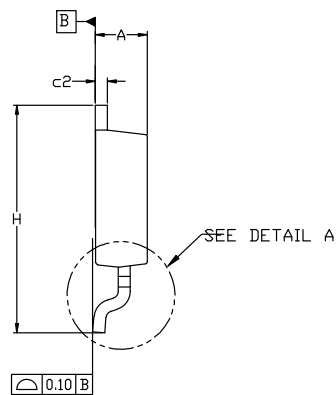
DATE 20 DEC 2023



NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

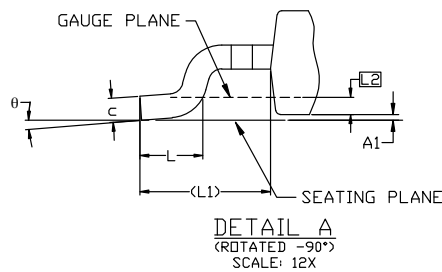
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.

D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

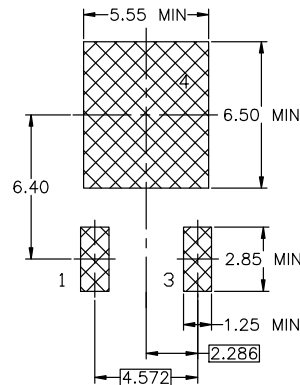
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.

F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

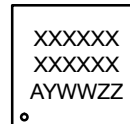
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TD228P991X239-3N.



DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	2.18	2.29	2.39
A1	0.00	—	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*


*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

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