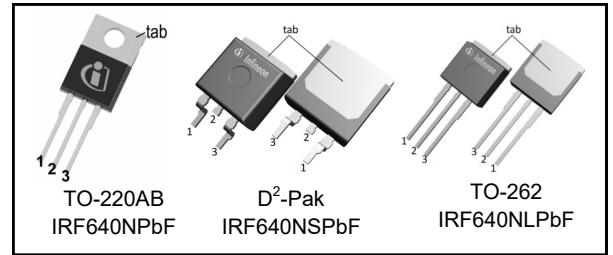
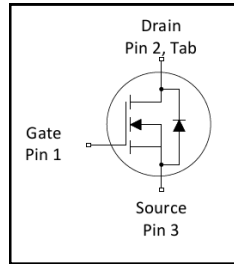


$V_{(BR)DSS}$	200V
$R_{DS(on)}$ max.	0.15Ω
I_D	18A

Features

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free



G	D	S
Gate	Drain	Source

Description

Fifth Generation HEXFET Power MOSFETs utilizes advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of other applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of TO-220 contributes to the wide acceptance throughout the industry.

The D² Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on resistance in any existing surface mount package. The D2 Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRF630NL) is available for low-profile application.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF640NPbF	TO-220	Tube	50	IRF640NPbF
IRF640NSPbF	D ² -Pak	Tape and Reel	800	IRF640NSPbF
IRF640NLPbF	TO-262	Tube	50	IRF640NLPbF

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	18	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	13	
I_{DM}	Pulsed Drain Current ①	72	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	150	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	247	mJ
I_{AR}	Avalanche Current ①	18	A
E_{AR}	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt⑥	8.1	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw④	10 lbf•in (1.1N•m)	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.15	Ω	$V_{GS} = 10V, I_D = 11A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Trans conductance	6.8	—	—	S	$V_{DS} = 50V, I_D = 11A$ ③
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Q_g	Total Gate Charge	—	—	67	nC	$I_D = 11A$ $V_{DS} = 160V$ $V_{GS} = 10V$ ④
Q_{gs}	Gate-to-Source Charge	—	—	11		
Q_{gd}	Gate-to-Drain Charge	—	—	33		
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 100V$ $I_D = 11A$ $R_G = 2.5\Omega$ $R_D = 9.0\Omega$ ③
t_r	Rise Time	—	19	—		
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		
t_f	Fall Time	—	5.5	—		
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1160	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$, See Fig.5
C_{oss}	Output Capacitance	—	185	—		
C_{rss}	Reverse Transfer Capacitance	—	53	—		

Diode Characteristics

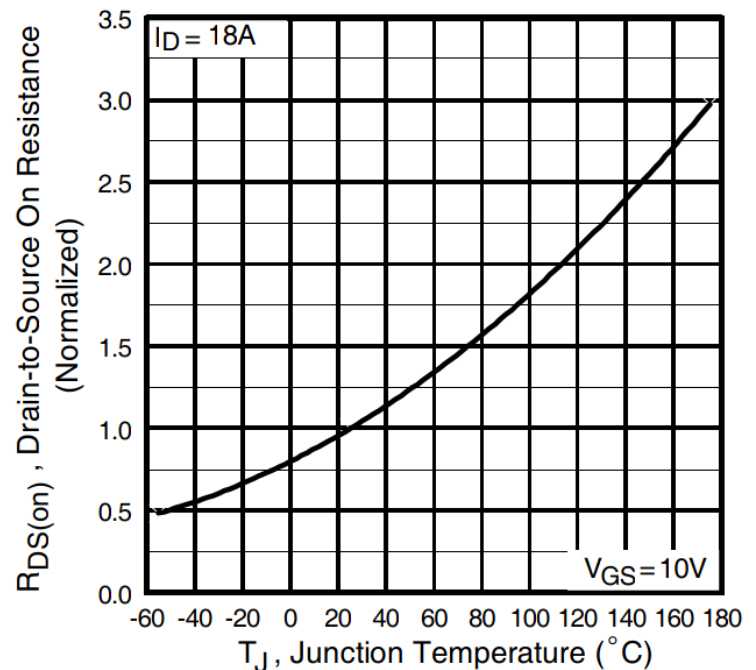
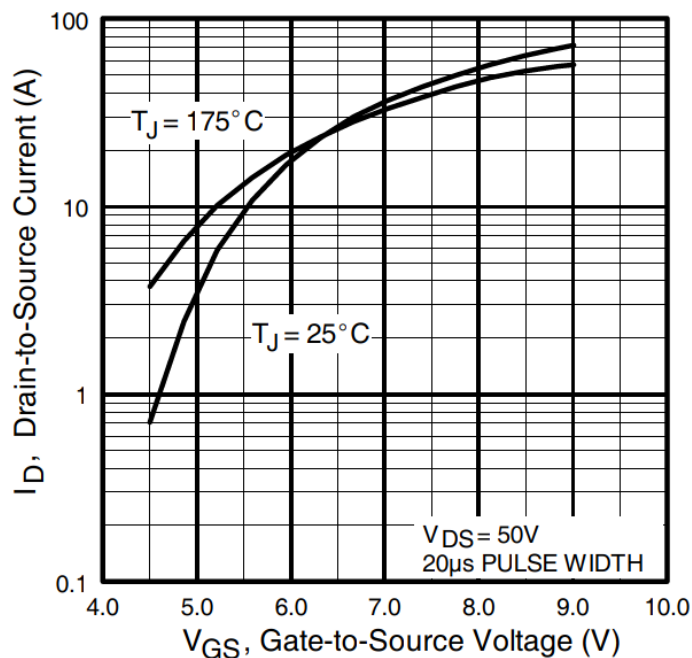
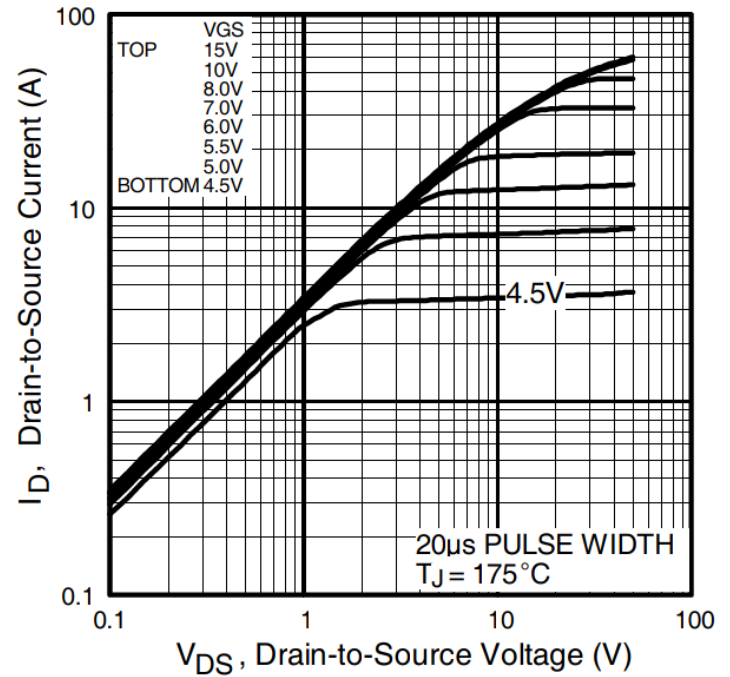
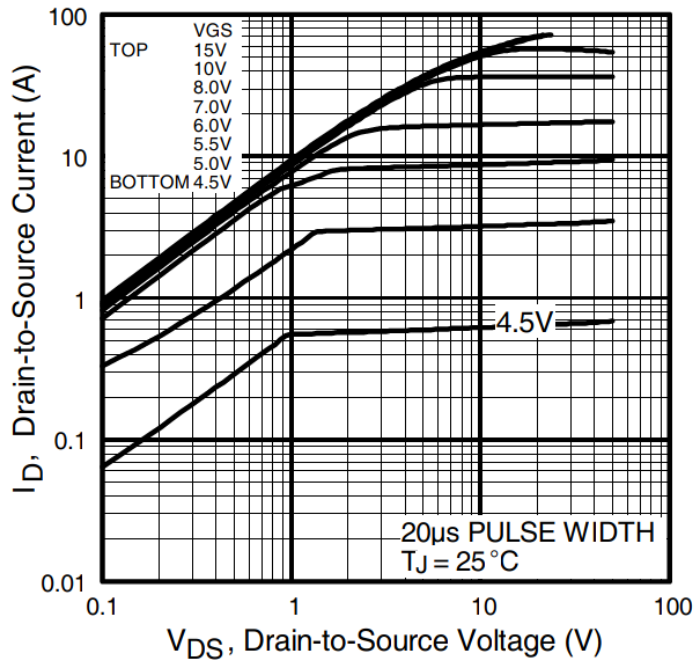
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	18	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	72		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 11A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	167	251	ns	$T_J = 25^\circ\text{C}, I_F = 11A,$
Q_{rr}	Reverse Recovery Charge	—	929	1394	nC	$di/dt = 100A/\mu s$ ③

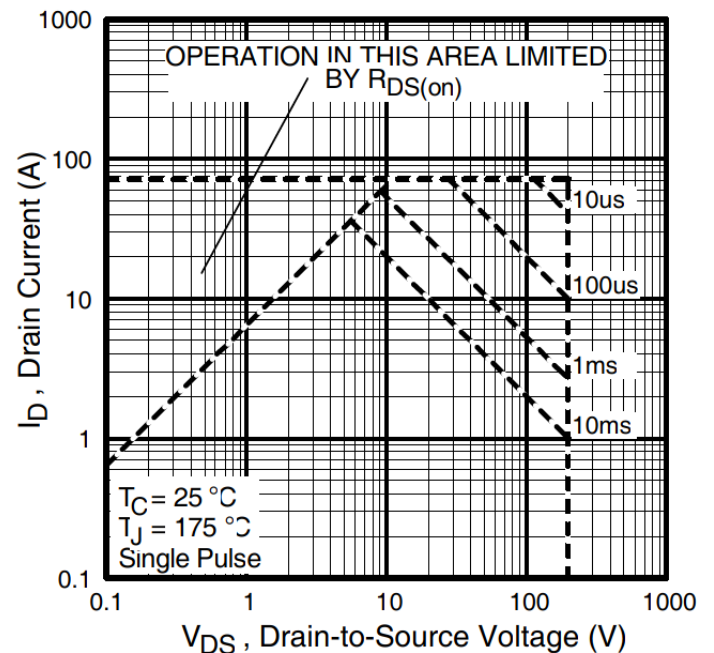
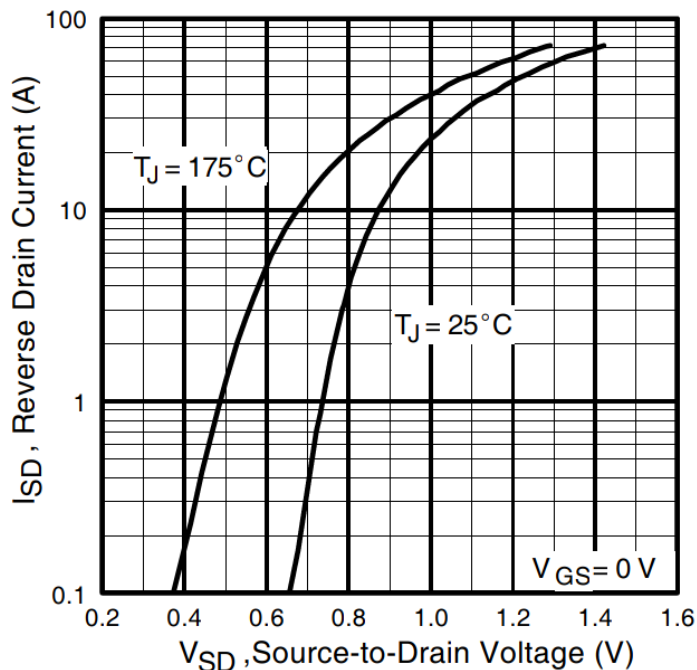
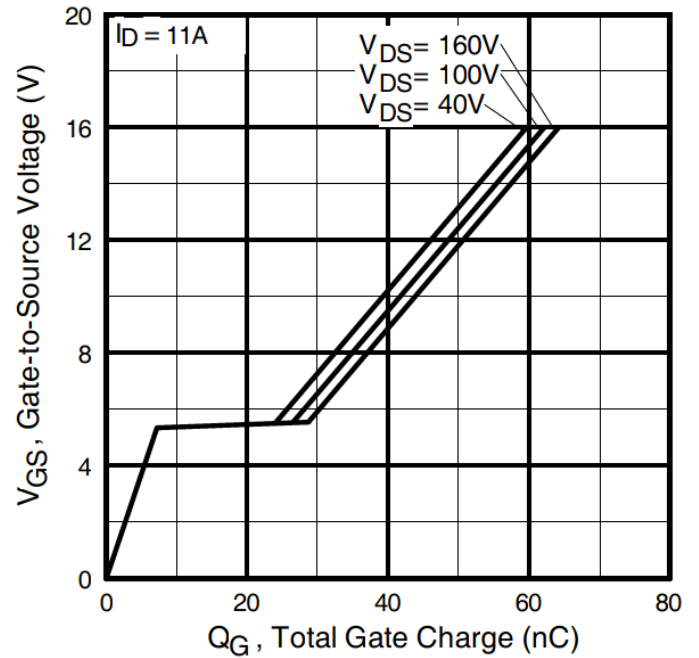
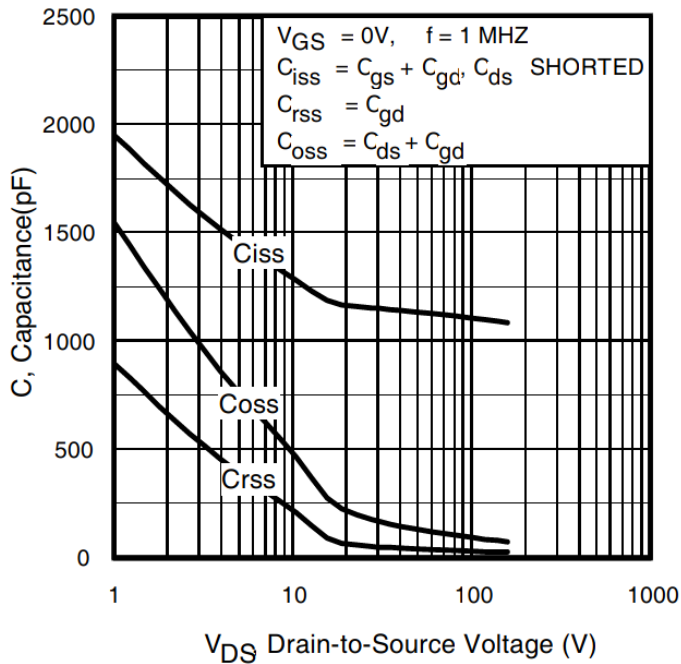
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ④	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑤	—	40	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting $T_J = 25^\circ\text{C}$, $L = 4.2mH$, $R_G = 25\Omega$, $I_{AS} = 11A$
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ This is only applied to -TO-220AB package.
- ⑤ This is applied to D2 Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note# [AN-994](#).
- ⑥ $I_{SD} \leq 11A$, $di/dt \leq 344A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.





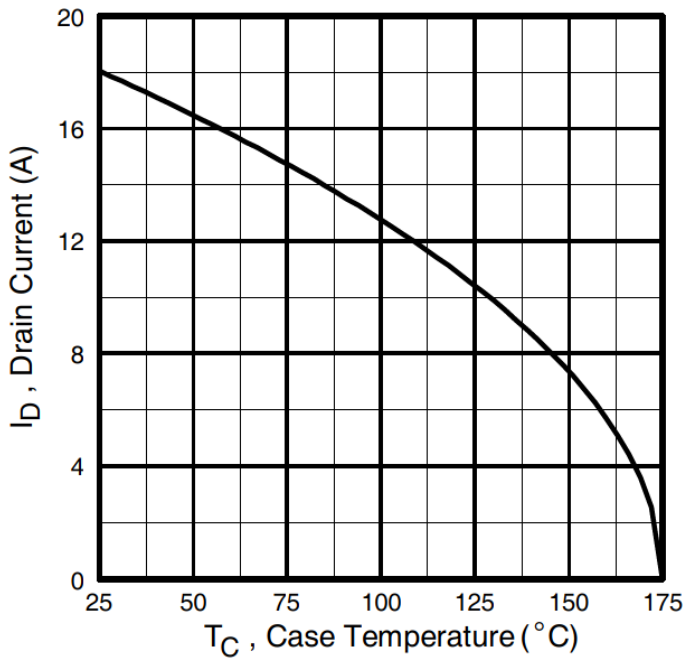


Fig 9. Maximum Drain Current vs. Case Temperature

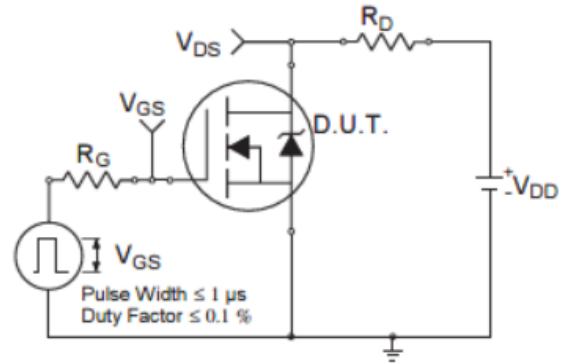


Fig 10a. Switching Time Test Circuit

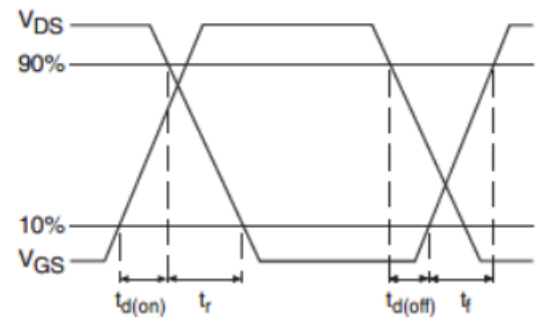


Fig 10b. Switching Time Waveforms

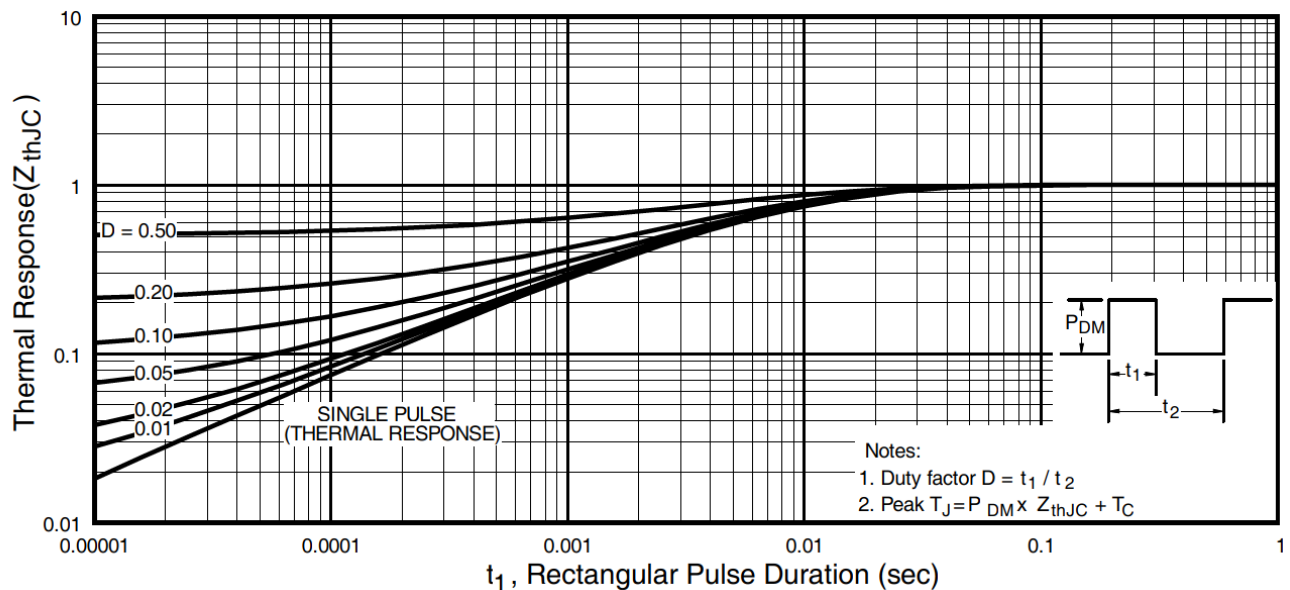


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

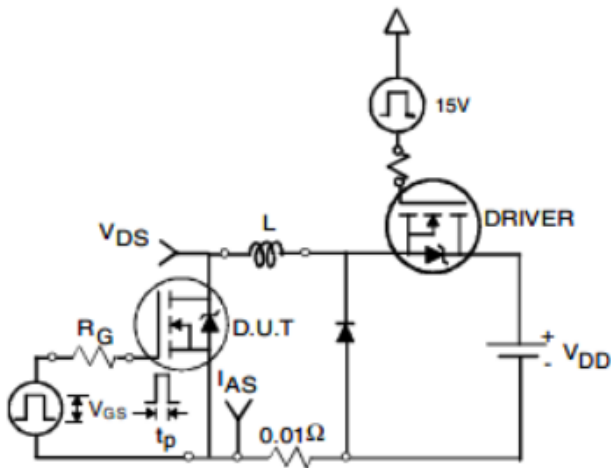


Fig. 12a. Unclamped Inductive Test Circuit

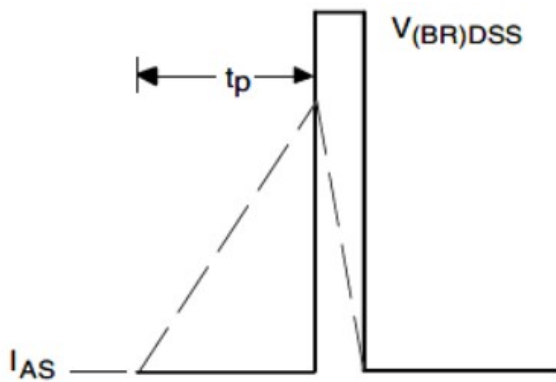


Fig. 12b. Unclamped Inductive Waveforms

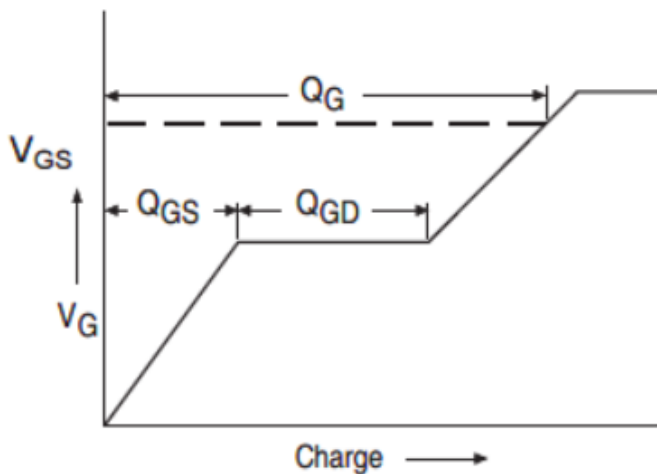


Fig 13a. Basic Gate Charge Waveform

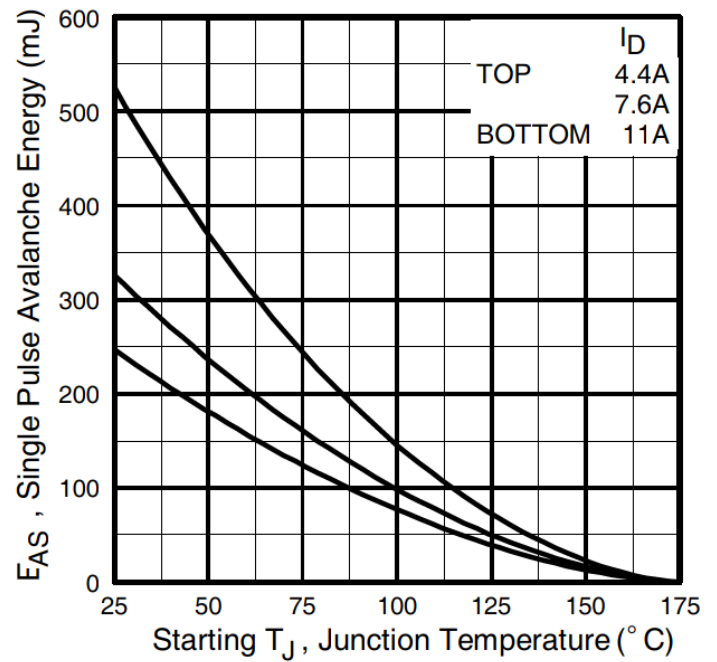


Fig 12c. Maximum Avalanche Energy vs. Drain Current

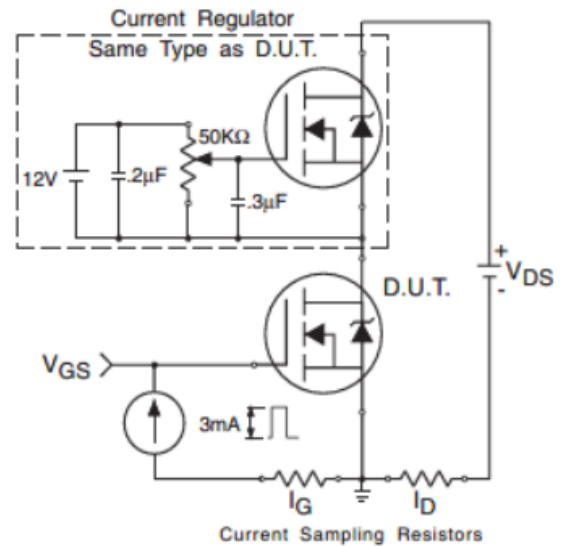
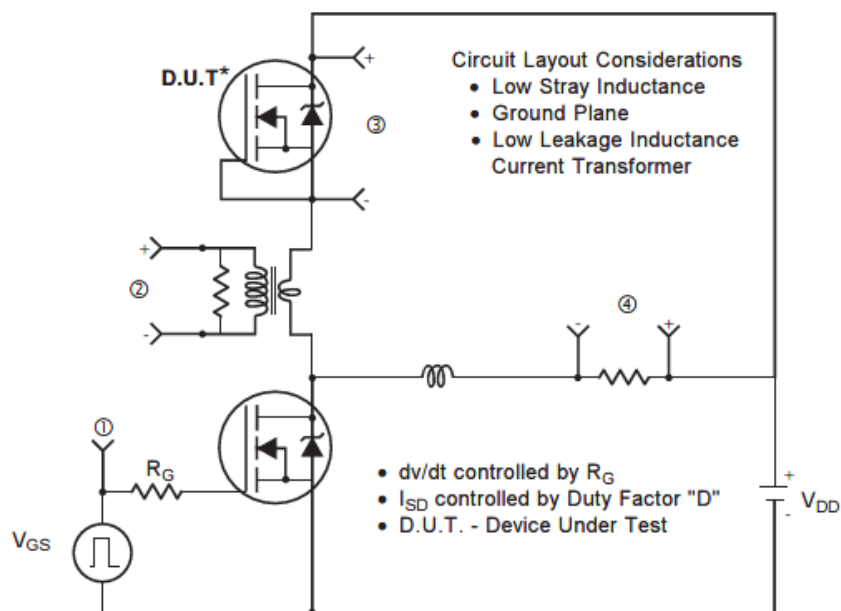


Fig 13b. Gate Charge Test Circuit



* Reverse Polarity of D.U.T for P-Channel

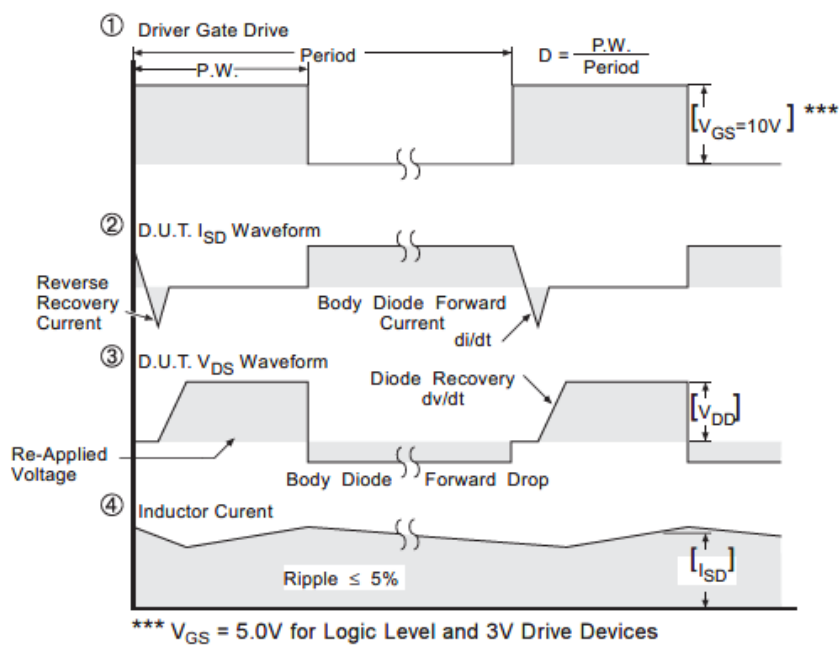
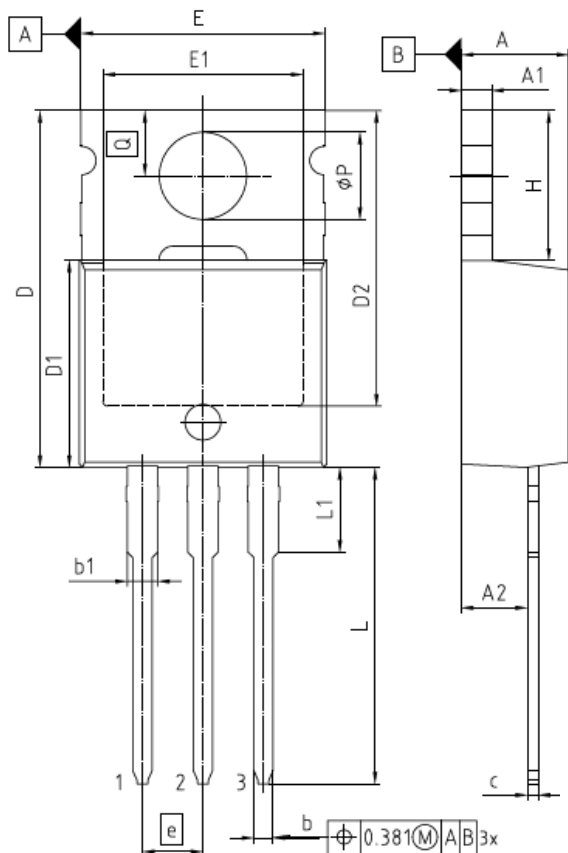


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

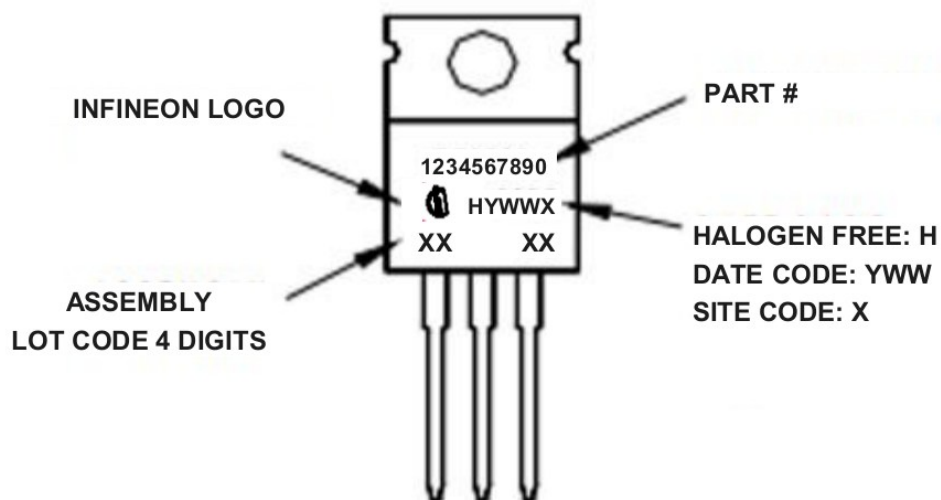
TO-220 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

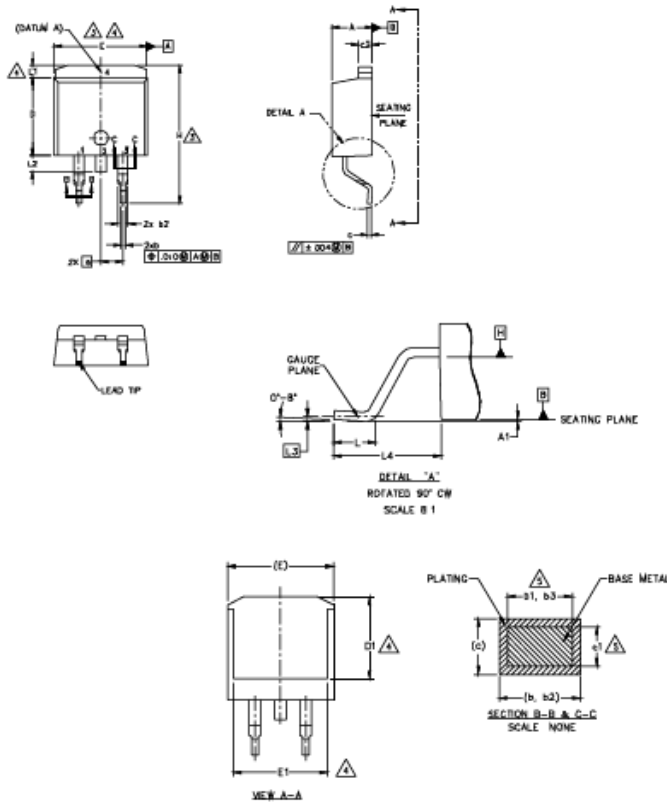
PACKAGE - GROUP NUMBER: PG-TO220-3-U05		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	3.56	4.83
A1	1.14	1.40
A2	2.03	2.92
b	0.38	1.01
b1	1.14	1.78
c	0.36	0.61
D	14.22	16.51
D1	8.38	9.20
D2	11.68	12.88
E	9.65	10.67
E1	6.86	8.89
e	2.54	
N	3	
H	5.84	6.86
L	12.70	14.73
L1	3.56	4.06
øP	3.54	4.08
Q	2.54	3.42

TO-220 Part Marking Information



TO-220 packages are not recommended for Surface Mount Application.

D² Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



LEAD ASSIGNMENTS

DIGITS

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	4
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

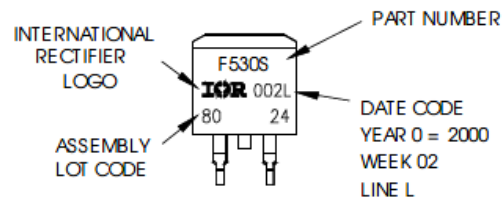
NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 (.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB

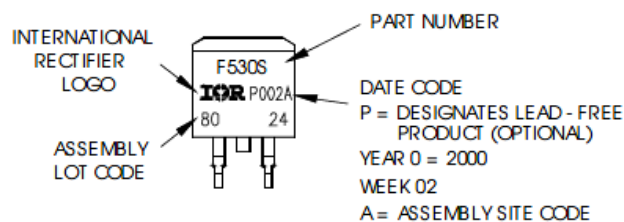
D² Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead - Free"



OR



[illegible]

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION INCH.
7. — OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYM BOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	
L2	3.56	3.71	.140	.146	4

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

Diagram illustrating the markings on a MOSFET package (IRL3103L):

- INTERNATIONAL RECTIFIER LOGO**: Points to the "IR" logo on the package.
- PART NUMBER**: Points to the "IRL3103L" marking.
- DATE CODE**: Points to the "719C" marking.
- YEAR 7 = 1997**: Indicates the year corresponding to the first digit of the date code.
- WEEK 19**: Indicates the week corresponding to the second and third digits of the date code.
- LINE C**: Indicates the line corresponding to the fourth digit of the date code.
- ASSEMBLY LOT CODE**: Points to the "17" marking.
- 89**: Points to the marking "89" on the package.

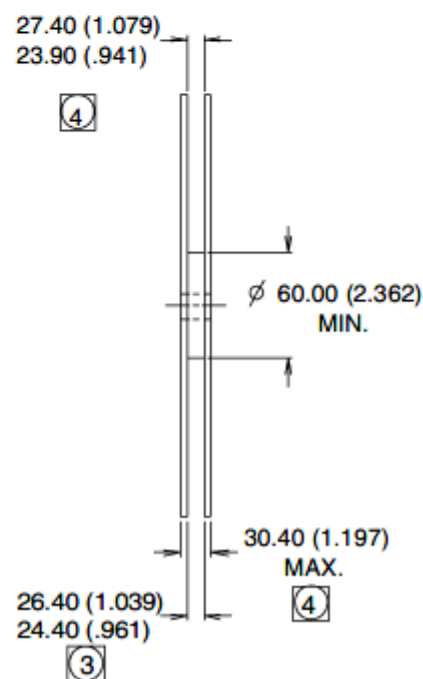
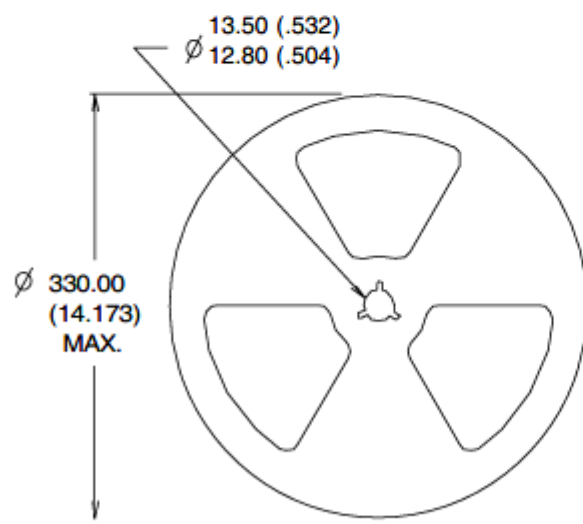
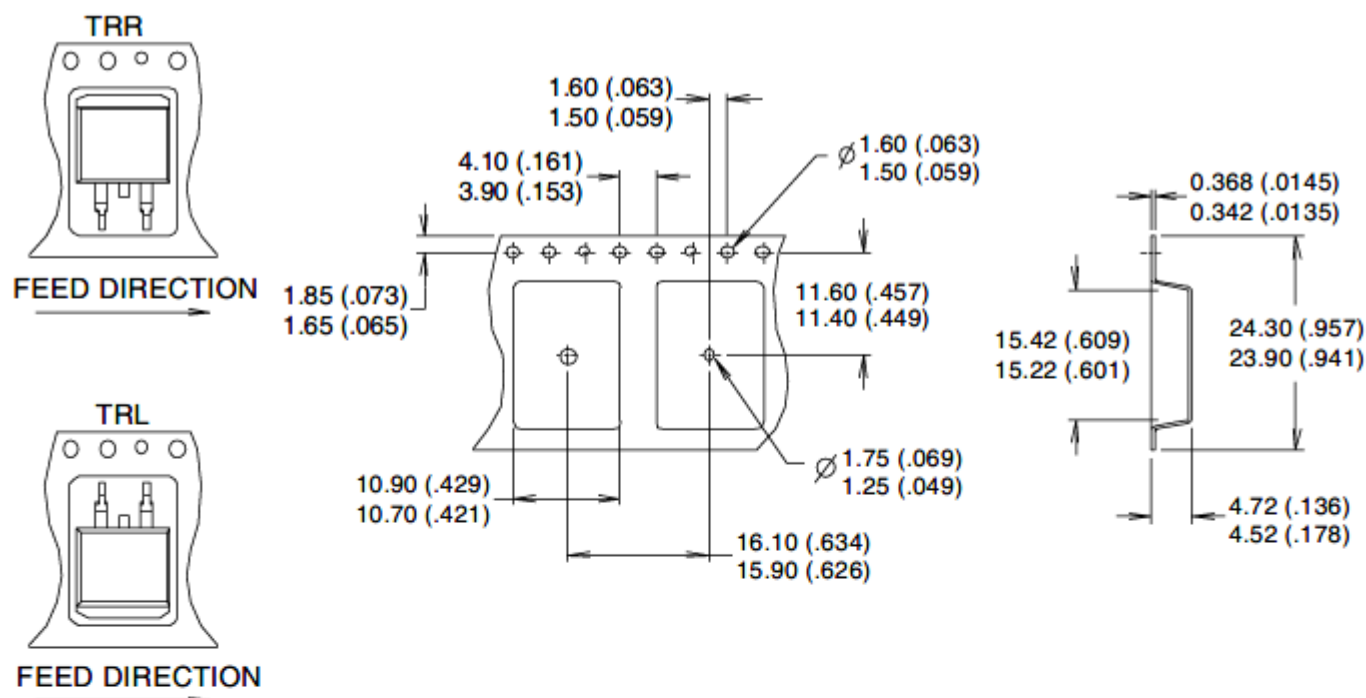
Diagram illustrating the marking on a MOSFET package (IRL3103L) with labels:

- PART NUMBER:** IRL3103L
- DATE CODE:** P719A
- ASSEMBLY SITE CODE:** 17 89

Additional markings and descriptions:

- INTERNATIONAL RECTIFIER LOGO:** IR
- ASSEMBLY LOT CODE:** 17
- DATE CODE:** P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
- YEAR 7 = 1997**
- WEEK 19**
- A = ASSEMBLY SITE CODE**

D² Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))



NOTES :

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Revision History

Date	Rev.	Comments
2026-07-27	2.1	- Update datasheet to Infineon format - Updated Package Outline and Part marking –page 8 - Added disclaimer on last page.

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